

## Analog Signal Input Class-D Amplifier for Piezo Speaker with DC-DC Converter

### ■ GENERAL DESCRIPTION

The NJW1263 is an analog signal input monaural class-D amplifier for Piezo speaker. And a built-in DC-DC converter generates variable output voltage (up to 20 V) with input voltage (3.0 to 4.2V).

The NJW1263 incorporates BTL amplifier, which eliminate AC coupling capacitors, and it is capable of driving Piezo speaker with simple external LC low-pass filters.

Class-D operation achieves lower power operation for Piezo speaker, thus the NJW1263 is suited for battery-powered applications.

### ■ PACKAGE OUTLINE

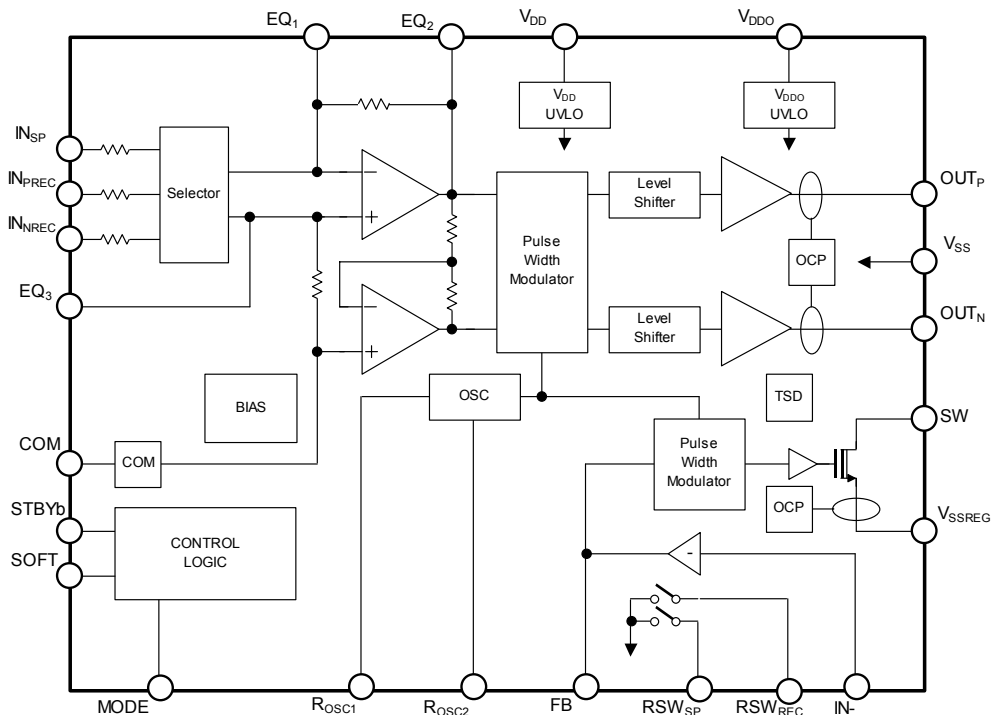


**NJW1263WLC1**

### ■ FEATURES

- Output Voltage  $V_{DD}=3.0V$  to  $4.2V$   
 $V_{DDO}=8.0$  to  $20.0V@SP$  MODE  
 $V_{DDO}=4.5V@REC$  MODE
- Analog Audio Signal Input
- 2input selector (Speaker Mode and Receiver Mode)
- 1-channel BTL Output, Piezo Speaker Driving
- Built-in DC-DC Converter
- Built-in Low Voltage Detector
- Standby (Hi-Z), Soft Start, Soft Mute Control
- Built-in Pop noise reduction
- Built-in Short Protector)
- Built-in Thermal Protection
- Package Outline: WCSP42

### ■ BLOCK DIAGRAM



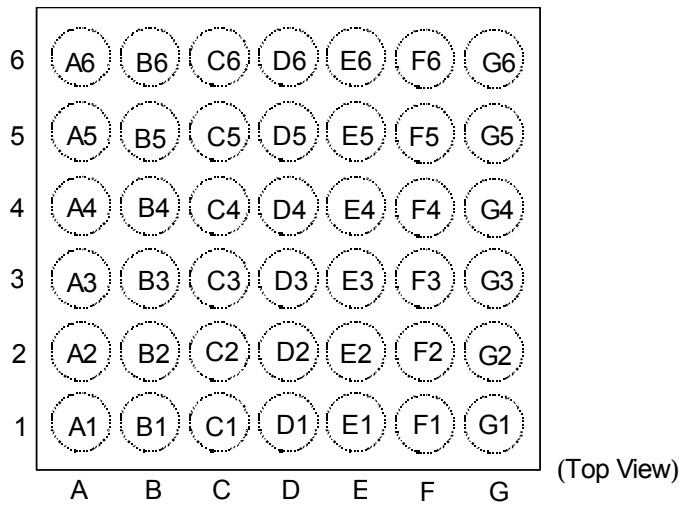
## ■ PIN CONFIGURATION

No.	SYMBOL	I/O	機能
A5	$V_{DD}$	-	Power supply: $V_{DD} = 3.7\text{ V}$
D5, D6	$V_{DDO}$	-	Output Power supply: $V_{DDO} = 8.0\text{ to }20.0\text{ V}$
F1	$IN_{SP}$	I	Noninverted signal input (SP Mode) terminal
G2	$IN_{PREC}$	I	Noninverted signal input (REC Mode) terminal
G3	$IN_{NREC}$	I	Inversion signal Input (REC Mode)
E1	$EQ_1$	I/O	LPF Setting terminal
E2	$EQ_2$	I/O	LPF Setting terminal
D1	$EQ_3$	I/O	LPF Setting terminal
G4	COM	I/O	Bias terminal
C3	SOFT	I/O	Capacitor connection terminal for soft start
F3	STBYb	I	Standby control terminal (STBYb = L: Standby)
E3	MODE	I	SP/REC mode switch terminal (MODE = H: SP Mode, MODE = L: REC Mode) The mode maintains the logic when the STBYb terminal is started up.
A4	$R_{OSC1}$	I/O	Resistance connection terminal for Class-D Amp.
F2	$R_{OSC2}$	I/O	Resistance connection terminal for switching regulator
A2, B3, B5, B6, C4 D4, E4, F4, F5, F6	$V_{SS}$	-	GND: $V_{SS} = 0\text{ V}$
E5, E6	$OUT_P$	O	Noninverted signal output terminal
C5, C6	$OUT_N$	O	Inversion signal output terminal
A1, B1, B2	SW	O	Inductor connection terminal
C1, C2	$V_{SSREG}$	-	GND: $V_{SSREG} = 0\text{ V}$
B4	IN-	I/O	Resistance connection terminal for DC/DC
A3	FB	I/O	Phase compensating device connection terminal for switching regulator
G5	$RSW_{REC}$	I/O	Resistance connection terminal to adjust DC/DC
D2	$RSW_{SP}$	I/O	Resistance connection terminal to adjust DC/DC
D3	TEST1	I	Test Pin (50k $\Omega$ ground) Should be floating or $V_{SS}$ fixation.
A6, G1, G6	NC	-	NC pin Should be floating or $V_{SS}$ fixation.

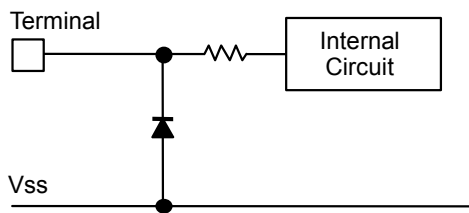
Note:  $V_{BAT} = V_{DD}$

Note: Do not do floating the input terminal.

## ■ TERMINAL CONFIGURATION



## INPUT TERMINAL



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply Voltage	V <sub>DD</sub> V <sub>DDO</sub>	V <sub>DD</sub> V <sub>DDO</sub>	-0.3 to +5.5 -0.3 to +36	V
Input Voltage	V <sub>IN</sub>	IN <sub>SP</sub> , IN <sub>PREC</sub> , IN <sub>NREC</sub> , STBYb, IN <sup>-</sup> , RSW <sub>REC</sub> , RSW <sub>SP</sub> MODE	-0.3 to V <sub>DD</sub> +0.3	V
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-40 to +125	°C
Power Dissipation	P <sub>DMAX2</sub>	2 layers (EIAJ), T <sub>j</sub> = 125°C	610	mW
	P <sub>DMAX4</sub>	4 layers (EIAJ), T <sub>j</sub> = 125°C	1200	mW
Thermal resistance	θ <sub>ja2</sub>	2 layers (EIAJ), T <sub>j</sub> = 125°C	164.5	°C /W
	θ <sub>ja4</sub>	4 layers (EIAJ), T <sub>j</sub> = 125°C	81.8	°C /W

Note 1) All voltage are relative to “V<sub>SS</sub> =0V” reference.

Note 2) The LSI must be used within the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI. Mounted on 2-layer/ 4-layer board based on EIA/JEDEC

Note 3) The IC must be used inside of the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

Note 4) De-coupling capacitors must be connected between each power supply terminal and GND (V<sub>DD</sub>-V<sub>SS</sub>, V<sub>DDO</sub>-V<sub>SS</sub>).

Note 5) The maximum power dissipation in the system is calculated, as shown below.

$$P_{DMAX} = \frac{T_{jMAX} [^{\circ}C] - T_a [^{\circ}C]}{\theta_{ja} [^{\circ}C/W]}$$

Pdmax: Maximum Power Dissipation, Tjmax: Junction Temperature = 125°C

Ta: Ambient Temperature, θja: Thermal Resistance of package = 164.5°C/W

$$P_d = \frac{125 - 50}{164.5 /W} = 456[mW]$$

Note 6 ) The W-CSP package must not be illuminated by light because the characteristic may be affected by the photoelectric effect.

## ■ ELECTRICAL CHARACTERISTICS

### ● DC Characteristics

$T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.7\text{ V}$ ,  $V_{DDO} = 13.0\text{ V}$  (SP Mode:  $R_{SW} = 180\text{ k}\Omega$ ,  $R_{SP} = 15\text{ k}\Omega$ )

$V_{DDO} = 4.5\text{ V}$  (REC Mode:  $R_{SW} = 180\text{ k}\Omega$ ,  $R_{REC} = 51\text{ k}\Omega$ ),  $V_{SS} = 0.0\text{ V}$ , Load Impedance =  $1.5\text{ }\mu\text{F}$

$R_{OSC1} = 82\text{ k}\Omega$ ,  $R_{OSC2} = 82\text{ k}\Omega$ ,  $C_{LPF} = 330\text{ pF}$ ,  $C_c = 0.033\text{ }\mu\text{F}$ , Output Filter: [ $L_{OUT} = 22\text{ }\mu\text{H}$ ,  $R_{DAMP} = 3.9\text{ }\Omega$ ]

SW regulator: [ $L_{SW} = 6.8\text{ }\mu\text{H}$ ,  $C_{SW} = 20\text{ }\mu\text{F} + 0.1\text{ }\mu\text{F}$ ,  $C_{cmpn1} = 10\text{ nF}$ ,  $C_{cmpn2} = 33\text{ pF}$ ,  $R_{cmpn} = 33\text{ k}\Omega$ ]

Input Signal:  $I_{N_{SP}} = 100\text{ mVrms}$ ,  $I_{N_{PREC}} - I_{N_{NREC}} = 100\text{ mVrms}$ , Input Frequency =  $1\text{ kHz}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD}, V_{DDO}$ Supply Voltage	$V_{DD}$		3.0	3.7	4.2	V
	$V_{DDO}$	SP Mode	8.0	13.0	20.0	V
		REC Mode	4.2	4.5	4.8	V
Output Driver On-state Resistance (High-side)	$R_{ONHSP}$	SP Mode, $OUT_P, OUT_N$ $V_{OUTP,N} = V_{DDO} - 0.1\text{ V}$	1.3	2.0	2.4	$\Omega$
	$R_{ONHREC}$	REC Mode, $OUT_P, OUT_N$ $V_{OUTP,N} = V_{DDO} - 0.1\text{ V}$	1.3	2.2	2.8	$\Omega$
Output Driver On-state Resistance (Low-side)	$R_{ONLSP}$	SP Mode, $OUT_P, OUT_N$ $V_{OUTP,N} = 0.1\text{ V}$	1.3	2.0	2.4	$\Omega$
	$R_{ONLREC}$	REC Mode, $OUT_P, OUT_N$ $V_{OUTP,N} = 0.1\text{ V}$	1.3	2.2	2.8	$\Omega$
Switching Regulator Output Driver On-state Resistance	$R_{ONSW}$	SW $V_{SW} = 0.1\text{ V}$	0.05	0.4	0.7	$\Omega$
Input Impedance	$R_{INSP}$	$I_{N_{SP}}$	90	120	150	k $\Omega$
	$R_{INPREC}$	$I_{N_{PREC}}$	180	240	300	k $\Omega$
	$R_{INNREC}$	$I_{N_{NREC}}$	280	360	440	k $\Omega$
Operating Current (Standby)	$I_{ST}$	STBYb: "L", No Load	-	-	1	$\mu\text{A}$
Operating Current (No signal input)	$I_{BATSP}$	SP Mode, Non-LC Filter, No Load	-	13.0	16.5	mA
	$I_{BATREC}$	REC Mode Non-LC Filter, No Load	-	4.0	5.0	mA

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	$V_{IH}$	STBYb,MODE Pin	1.5	-	$V_{DD}$	V
	$V_{IL}$	STBYb,MODE Pin	0	-	0.5	V
Input Leakage Current	$I_{LK}$	STBYb, MODE Pin	-	-	$\pm 1$	$\mu A$
SW Off Leak Current	$I_{LKSW}$	SW Pin	-	-	-	$\mu A$
OUT <sub>P</sub> Ground Resistance	$R_{OUTP}$	OUT <sub>P</sub> Pin	70	100	130	k $\Omega$
OUT <sub>N</sub> Ground Resistance	$R_{OUTN}$	OUT <sub>N</sub> Pin	70	100	130	k $\Omega$
Class-D Amplifier Oscillation Frequency	$f_{OSCD}$		180	250	320	kHz
Switching Regulator Oscillation Frequency	$f_{OSCSW}$		500	600	750	kHz
Soft Start Resistance	$R_{SST}$	SOFT Pin	35	50	65	k $\Omega$
Soft Mute Resistance	$R_{SMT}$	SOFT Pin	35	50	65	k $\Omega$
Start-up Time	$T_{ON}$		5.0	6.7	8.4	ms
Stop Time	$T_{OFF}$		10.0	13.3	16.6	ms
Class-D Amplifier Voltage Gain	$AV_{SP}$	SP Mode, No Load	-	27.6	-	dB
	$AV_{REC}$	REC Mode, No Load	-	5.1	-	dB
MODE Setup Time	$T_{STUP}$	Refer to Figure 1.	10	-	-	$\mu s$
MODE Holding Time	$T_{HLD}$	Refer to Figure 1.	50	-	-	$\mu s$

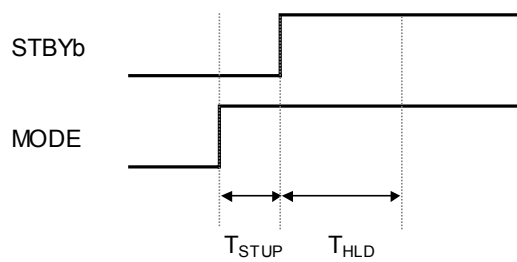


Figure 1: STBYb/MODE input timing

● AC Characteristics

$T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.7\text{ V}$ ,  $V_{DDO} = 13.0\text{ V}$  (SP Mode:  $R_{SW}=180\text{ k}\Omega$ ,  $R_{SP}= 15\text{ k}\Omega$ )

$V_{DDO} = 4.5\text{ V}$  (REC Mode:  $R_{SW}= 180\text{ k}\Omega$ ,  $R_{REC}= 51\text{ k}\Omega$ ),  $V_{SS} = 0.0\text{ V}$ , Load Impedance =  $1.5\text{ }\mu\text{F}$

$R_{OSC1}=82\text{ k}\Omega$ ,  $R_{OSC2}=82\text{ k}\Omega$ ,  $C_{LPF}= 330\text{ pF}$ ,  $C_c=0.033\text{ }\mu\text{F}$ , Output Filter: [ $L_{OUT}= 22\text{ }\mu\text{H}$ ,  $R_{DAMP}= 3.9\Omega$ ]

SW regulator: [ $L_{SW}= 6.8\text{ }\mu\text{H}$ ,  $C_{SW}= 20\text{ }\mu\text{F}+0.1\text{ }\mu\text{F}$ ,  $C_{cmpn1}= 10\text{ nF}$ ,  $C_{cmpn2}= 33\text{ pF}$ ,  $R_{cmpn}= 33\text{ k}\Omega$ ]

Input Signal:  $I_{N_{SP}}= 100\text{ mVrms}$ ,  $I_{N_{PREC}}= I_{N_{NREC}} = 100\text{ mVrms}$ , Input Frequency =  $1\text{ kHz}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD+N	THD+N <sub>SP</sub>	SP Mode, $V_{OUTSP} = 3\text{ Vrms}$	-	0.1	-	%
	THD+N <sub>REC</sub>	REC Mode $V_{OUTREC} = 1\text{ Vrms}$	-	0.05	-	%
Maximum Output Voltage	$V_{OUTSP}$	SP Mode, THD+N=1%	-	20	-	$V_{PP}$
	$V_{OUTREC}$	REC Mode, THD+N=1%	-	2.7	-	Vrms
S/N	SN	REC MODE, A-weight $V_{OUTREC} = 1\text{ Vrms}$	-	80	-	dB
Noise Floor	$V_N$	REC MODE, A-weight	-	100	-	$\mu\text{Vrms}$

## FUNCTIONAL DESCRIPTION

- Signal Input Terminal (IN<sub>SP</sub>, IN<sub>PREC</sub>, IN<sub>NREC</sub>)  
Analog signal input. The input signal is selected by the operational mode.
- Capacitor connection terminal for LPF (EQ1, EQ2, EQ3)  
The amount of current passing through a capacitive load increases proportionately with frequency of audio signal. Input filters should be put in the input line to reduce load current at high frequency-band. The input low pass filters are composed of feedback resistor (R<sub>1</sub>) and capacitor (C<sub>LPF</sub>).  
Refer to the following expression.

$$R_1 = 120\text{k}\Omega, C_{LPF} = 330\text{pF}$$

$$f_{LPF} = \frac{1}{2 R_1 C_{LPF}} = \frac{1}{2 \times 3.14 \times 120\text{k}\Omega \times 330\text{pF}} \quad 4.0[\text{kHz}]$$

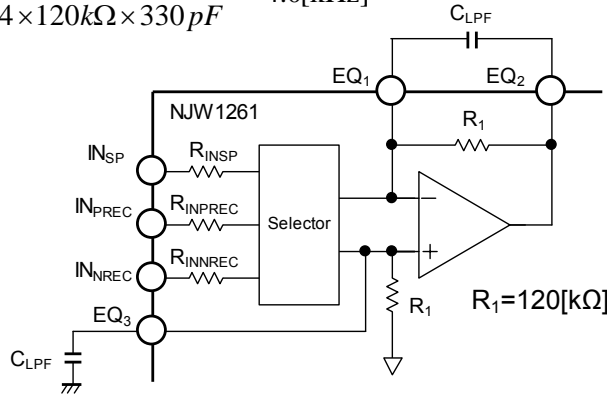


Figure 2: Input LPF composition

- Signal Output Terminal (OUT<sub>P</sub>, OUT<sub>N</sub>)  
The output signals are PWM signals, which will be converted to analog signal via external 2nd-order or higher LC filter. Should be connected to the damping resistor (R<sub>DAMP</sub>) between OUT<sub>P</sub> pin and coil, and between OUT<sub>N</sub> pin and coil to reduce the current consumption with signal-input close to cutoff-frequency of LPF (f<sub>c</sub>).  
Set the value of L<sub>OUT</sub>, C<sub>L</sub>, and R<sub>DAMP</sub> to become Q < 1.  
Refer to the following expression.

$$L_{OUT} = 22\mu\text{H}, C_L = 1.5\mu\text{F}, R_{DAMP} = 3.9\Omega, \text{Equivalent direct resistance of L (} R_{DCR} \text{)} = 0.5\Omega$$

$$f_c = \frac{1}{2 \sqrt{2 L_{OUT} C_L}} = \frac{1}{2 \times 3.14 \times \sqrt{2 \times 22\mu\text{H} \times 1.5\mu\text{F}}} \quad 19.6[\text{kHz}]$$

$$Q = \frac{1}{R_{DAMP} + R_{DCR}} \sqrt{\frac{L_{OUT}}{2 C_L}} = \frac{1}{3.9 + 0.5} \times \sqrt{\frac{22\mu\text{H}}{2 \times 1.5\mu\text{F}}} \quad 0.61$$



- Standby Terminal (STBYb)

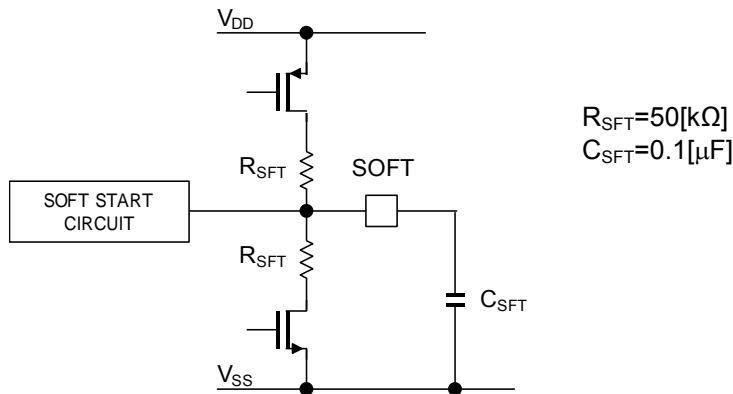
By setting the STBYb pin to “L” level, it switches the NJW1261 into standby condition. During the standby condition, output pins (OUT<sub>P</sub>, OUT<sub>N</sub>, SW) become high impedance and class-D amplifier output is connected with V<sub>SS</sub> with about 100kΩ. Keep the STBYb pin to “L” level at least 13.3ms once switched into the standby condition.

For normal operation, the STBYb pin requires “H” level. Time from the standby release to class-D power amplifier operation is 6.7ms(TYP). Do not change to the standby mode until the power amplifier operation.

Set the standby mode at power supply ON/OFF.

- Capacitor connection terminal for soft start (SOFT)

Capacitor connection terminal for soft start and soft mute



- Step-up switching regulator

The switching regulator is used as power supply (V<sub>DDO</sub>) for power amplifier of class-D. The PFM controlled switching regulator works with external components, which are coil, capacitor, Schottky barrier diode and step-up voltage setting resistance.

● Mode

SP/REC mode selection terminal. The output power-supply voltage, the input selector, and the voltage gain change when the mode is switched.

MODE="H":SP (Speaker) Mode    Audio input terminal: IN<sub>SP</sub>(Shingle end input)  
 Class-D amplifier output power-supply voltage: Step-up switching regulator

$$V_{SWSP} = 1.0V \times \left( 1 + \frac{R_{SW}}{R_{SP}} \right)$$

$R_{SW} + R_{SP} = 100 \text{ Kohm to } 1300 \text{ Kohm.}$

Voltage gain: 27.6 dB (TYP)

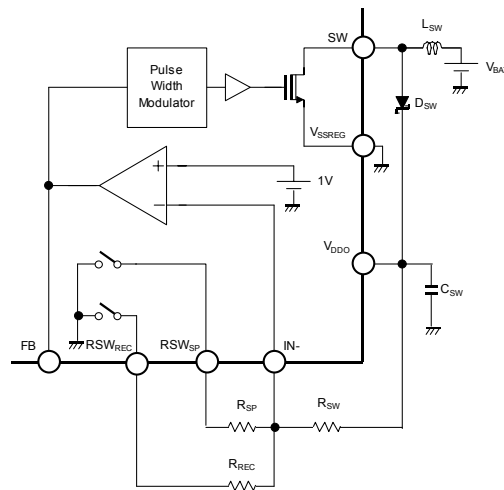
MODE="L":REC (Receiver) Mode    Audio input terminal: IN<sub>PREC</sub>, IN<sub>NREC</sub>(Difference input)  
 Class-D amplifier output power-supply voltage: Step-up switching regulator

$$V_{SWREC} = 1.0V \times \left( 1 + \frac{R_{SW}}{R_{REC}} \right)$$

Set the 4.5V(TYP) DC/DC voltage by  $R_{SW}$  and  $R_{SP}$ .

$R_{SW} + R_{SP} = 100 \text{ Kohm to } 1300 \text{ Kohm.}$

Voltage gain: 5.1 dB (TYP)



**Switching regulator circuit**

Note) Set the Step-up switching regulator voltage within the range of the V<sub>DD0</sub> operation voltage.

Note) Reset it when you switch MODE. (STBYb"L")

● Low Voltage Detector

When the power-supply voltage drops down to below V<sub>DD</sub>, the output driver is turned off output pins (OUT<sub>P</sub>, OUT<sub>N</sub>, SW) become high impedance and class-D amplifier output is connected with V<sub>SS</sub> with about 100kΩ.

## ● Short Circuit Protection

The short-circuit protection circuit operates at the condition of the following.

- Short between  $OUT_P$  and  $OUT_N$
- Power supply short and earth fault of  $OUT_P$  terminal
- Power supply short and earth fault of  $OUT_N$  terminal
- Power supply short of SW terminal

When  $OUT_P$  and  $OUT_N$  of the short-circuit protection circuit operates, the  $OUT_P$  and  $OUT_N$  become high impedance and class-D amplifier output is connected with  $V_{SS}$  with about 100k $\Omega$ . It restarts by pulse-by-pulse of built-in clock of class-D amplifier.

When SW terminal of the short-circuit protection circuit operates, the SW terminal become high impedance and class-D amplifier output is connected with  $V_{SS}$  with about 100k $\Omega$ . It restarts by pulse-by-pulse of built-in clock of the switching regulator.

Note)

\*1 The detectable current and the period for the protection depend on the power supply voltage, chip temperature and ambient temperature.

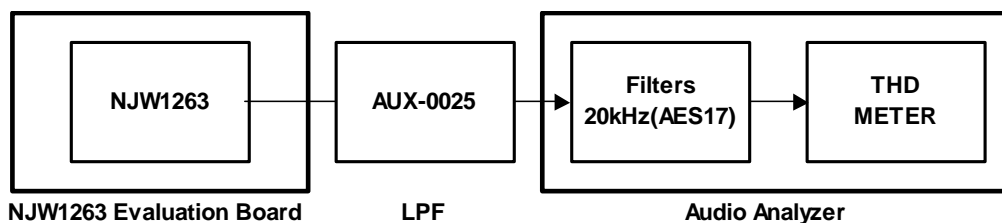
\*2 The short protector is not effective for a long term short-circuit current but for an instantaneous accident. Continuous high current may cause permanent damage to the NJW1261.

## ● Thermal protection

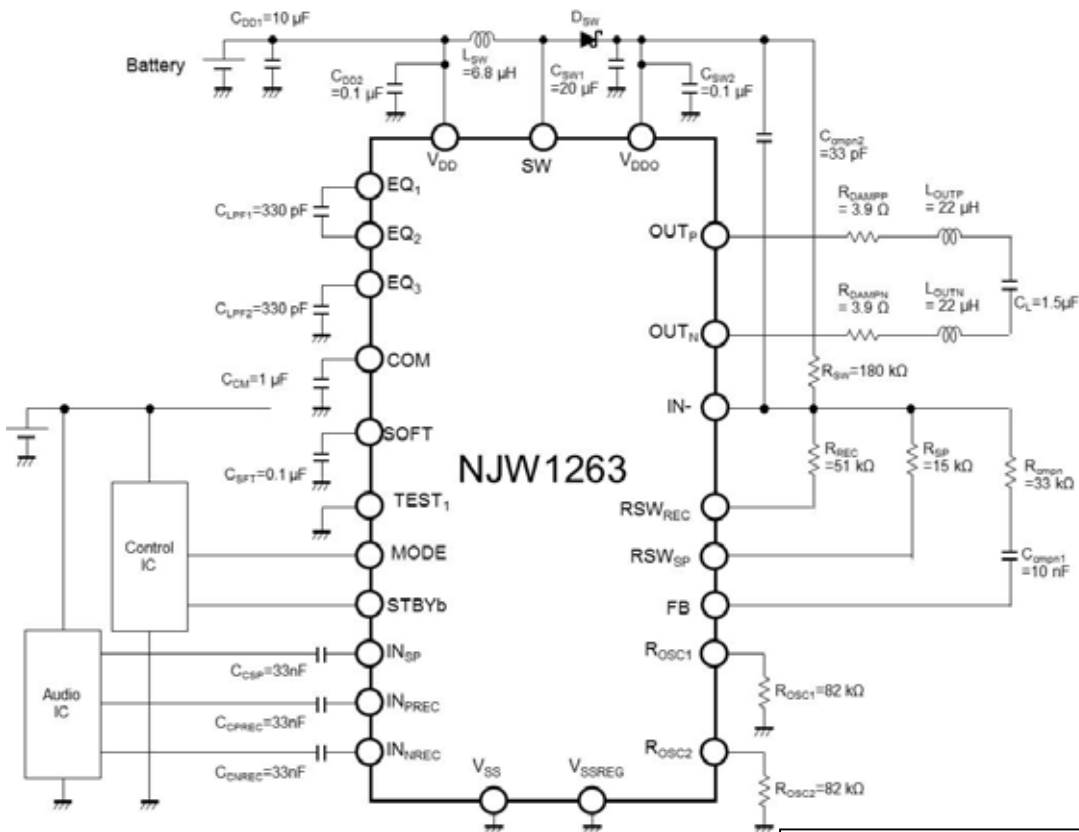
When the junction temperature is more than specified value, the output driver is turned off output pins ( $OUT_P$ ,  $OUT_N$ , SW) become high impedance and class-D amplifier output is connected with  $V_{SS}$  with about 100k $\Omega$ .

When the junction temperature is less than specified value, protection is released.

## ■ TOTAL HARMONIC DISTORTION MEASUREMENT CIRCUIT



## ■ TYPICAL APPLICATION CIRCUIT



### ■ Recommended Parts

CDD1: GRM31CB31E106KA75L(muRata)  
 CSW1: GRM31CB31E106KA75L(muRata) x 2  
 CDD2, CSW2, CSFT: GRM155B31E104KA87D(muRata)  
 CCM: GRM155B31A105KE15D(muRata)  
 CCS, CCPREC, CCNREC: GRM033B10J333KE01D(muRata)  
 Ccmpn1: GRM155R11C103KA01D(muRata)  
 Ccmpn2: GRM155C1H330JA01D(muRata)  
 CLPF1, CLPF2: GRM155B11H331KA01D(muRata)  
 LSW: LQH44PN6R8MPO(muRata)  
 LOUTP, LOUTN: LQH44PN220MP0(muRata)  
 DSW: RSX201VA-30(ROAM)  
 RDAMP: ERJ-14YJ3R9U(Panasonic)

### ■ Specified Parts

Rosc1, Rosc2: RK73H1JTDD8202F(KOA)

Note) De-coupling capacitors must be connected between each power supply terminal and GND ( $V_{DD}-V_{SS}$ ,  $V_{DDO}-V_{SS}$ ).

Note)  $V_{SS}$  should be connected at a nearest point to the IC on PCB.

Note)  $IN_{SP}$ ,  $IN_{PREC}$ ,  $IN_{NREC}$ ,  $EQ_1$ ,  $EQ_2$  and  $EQ_3$  should be not designed near  $OUT_P$ ,  $OUT_N$  and SW, which emit PWM noise.

Note) The transition time for MODE and STBYb signals must be less than 100 $\mu$ s. Otherwise, a malfunction may be occurred.

Note) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please test the circuit carefully to fit your application.

Note) RDAMP includes the resistance of the current limitation series of the piezoelectric element and the direct current resistance of coil LOU. Decide the value of RDAMP considering the piezo and the value of the coil.

Note) The speaker should be designed at a near the IC.

### [CAUTION]

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