General Description

The DSP-1K Audio Processor is a fast, low cost digital signal processor optimized for signal filtering, equalization and dynamics processing. Large word size provides easy, accurate algorithm creation for audio and other high dynamic range applications.

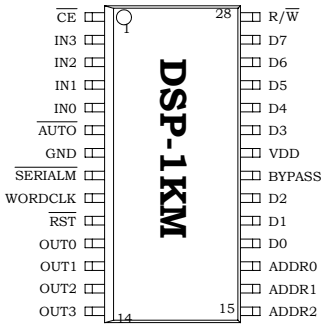
The DSP-1KM (AL3101) supports three control interface methods – serial, parallel, and auto-load. The DSP-1KS (AL3102) supports only the serial micro-interface.

Features

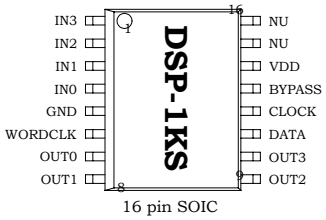
- High-speed, low-cost audio DSP engine
- Internal regulator allows operation at 3.3V or 5.0V
- Internal PLL – user need only supply WORDCLK at the desired sample rate
- 1024 instructions per word clock (49.152 MIPS @ 48KHz)
- Single cycle instruction execution
- Log and anti-log instructions
- Single cycle calculate and move
- Internal sample and program RAM
- 4 stereo inputs and outputs
- Parallel and serial micro-interfaces
- Stand alone operation with serial PROM

Applications

	Functions					
Products	**EQ**	**Dynamics Processing**	**Effects**	**Mixing/ Routing**	**Crossover**	**Psycho-acoustics**
Mixers	√	√		√		
Outboard processors	√	√	√	√		√
"Stomp" boxes	√	√	√			
Guitar amps		√	√			
Synthesizers			√	√		
Karaoke	√	√	√	√		√
Active speakers	√				√	√
DJ	√	√	√	√		



28 pin SOIC
300 mils wide



16 pin SOIC
300 mils wide

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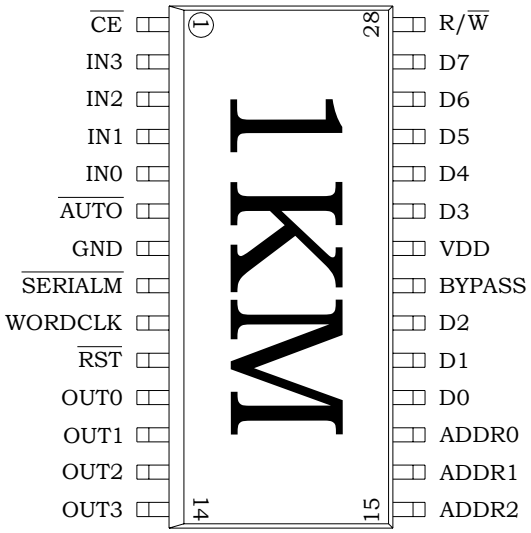
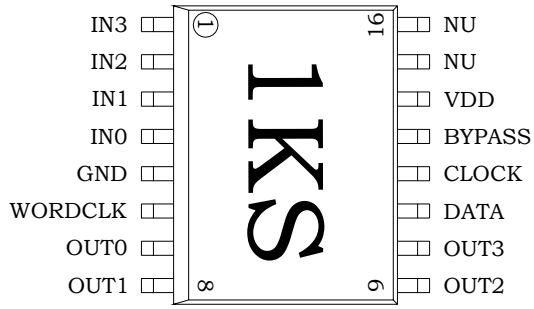
Pin descriptions



28 pin SOIC
300 mils wide



16 pin SOIC
300 mils wide

Pin Descriptions (1KS – 16-pin package)

(* Pullup to VDD via nom 30K † Pulldown to GND via nom. 30K)

Pin #	Name	Direction	Description
1	IN3	In	Serial input channels 6&7
2	IN2	In	Serial input channels 4&5
3	IN1	In	Serial input channels 2&3
4	IN0	In	Serial input channels 0&1
5	GND	In	Ground
6	WORDCLK	In	Word clock input, PLL uses this input to derive other signals
7	OUT0	Out	Serial output channels 0&1
8	OUT1	Out	Serial output channels 2&3
9	OUT2	Out	Serial output channels 4&5
10	OUT3	Out	Serial output channels 6&7
11	DATA	I/O*	Serial data to/from host
12	CLOCK	In†	Clock for serial data
13	BYPASS	I/O	Connect capacitor for internal regulator to this pin. Typ 0.1µF
14	VDD	In	VDD
15	NC	None	No internal connection. For future compatibility, do not connect to this pin.
16	NC	None	No internal connection. For future compatibility, do not connect to this pin.

Pin Descriptions (1KM – 28-pin package)

(* Pullup to VDD via nom 30K † Pulldown to GND via nom. 30K)

Pin #	Name	Direction	Description
1	CE	In*	Active low chip enable. If low, device is selected.
2	IN3	In	Serial input channels 6&7
3	IN2	In	Serial input channels 4&5
4	IN1	In	Serial input channels 2&3
5	IN0	In	Serial input channels 0&1
6	AUTO	In*	If low, loads code from external serial PROM. If high, enables micro interface.
7	GND	In	Ground
8	SERIAL M	In*	If low, uses serial micro interface, if high uses parallel micro interface or EPROM
9	WORDC LK	In	Word clock input, PLL uses this input to derive other signals
10	RST	In*	Active low reset. If low chip is being reset.
11	OUT0	Out	Serial output channels 0&1
12	OUT1	Out	Serial output channels 2&3
13	OUT2	Out	Serial output channels 4&5
14	OUT3	Out	Serial output channels 6&7
15	ADDR2	In*	Address bit 2
16	ADDR1	In*	Address bit 1
17	ADDR0	In*	Address bit 0
18	D0	I/O*	Data I/O 0 (Data in serial micro mode)
19	D1	I/O†	Data I/O 1 (Clock in serial micro mode)
20	D2	I/O*	Data I/O 2
21	BYPASS	I/O	Connect capacitor for internal regulator to this pin. Typ 0.1µF
22	VDD	In	VDD
23	D3	I/O*	Data I/O 3
24	D4	I/O*	Data I/O 4
25	D5	I/O*	Data I/O 5
26	D6	I/O*	Data I/O 6
27	D7	I/O*	Data I/O 7
28	R/W	In*	Read/Write. A low places the chip in write mode, a high in read

Electrical Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
Recommended Operating Conditions						
VDD	Supply	Note 1	4.75/3.15	5.0/3.3	5.25/3.45	V
IDD	Supply Current	Note 2		37/31		mA
GND	Ground			0		V
Fs	Sample rate		30	48	50	kHz
Temp	Temperature		0		70	°C
Inputs *(AUTO, SERIALM, ADDR2-0, D7-2, D0) These pins have an internal 30KΩ pull-up*						
V_{IH}	Logical "1" input voltage		2.4	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.8	V
V_T	Logic threshold			1.6		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current	V_{DD} = 5V		167	333	µA
Inputs *(CE, RST, R/W) These are Schmitt trigger inputs with an internal 30KΩ pull-up*						
V_{IH}	Logical "1" input voltage		2.5	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.5	V
V_{TR}	Rising logic threshold			2.0		V
V_{TF}	Falling logic threshold			1.0		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current	V_{DD} = 5V		167	333	µA
Inputs *(D1) This pin has an internal 30KΩ pull down*						
V_{IH}	Logical "1" input voltage		2.4	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.5	V
V_T	Logic threshold			1.6		V
I_{IH}	Logical "1" input current	V_{IH} = 5V			333	µA
I_{IL}	Logical "0" input current				2	µA
Inputs *(IN3 - 0)*						
V_{IH}	Logical "1" input voltage		2.4	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.8	V
V_T	Logic threshold			1.6		V
I_{IH}	Logical "1" input current	V_{IH} = 5V			2	µA
I_{IL}	Logical "0" input current				2	µA
Inputs *(WORDCLK) This pin is a Schmitt trigger input*						
V_{IH}	Logical "1" input voltage		2.5	.	VDD	V
V_{IL}	Logical "0" input voltage		GND	.	0.5	V
V_{TR}	Rising logic threshold			2.0		V
V_{TF}	Falling logic threshold			1.0		V
I_{IH}	Logical "1" input current				2	µA
I_{IL}	Logical "0" input current				2	µA

Outputs *(OUT3-0,D7-0)*

V_{OH}	Logical "1" output voltage	Unloaded		VDD		V
V_{OL}	Logical "0" output voltage	Unloaded		GND		V
I_{OH}	Logical "1" output current	V_{DD} = 5V V_O = 4.5V	-8.0			mA
I_{OL}	Logical "0" output current	V_{DD} = 5V V_O = 0.4V	8.0			mA

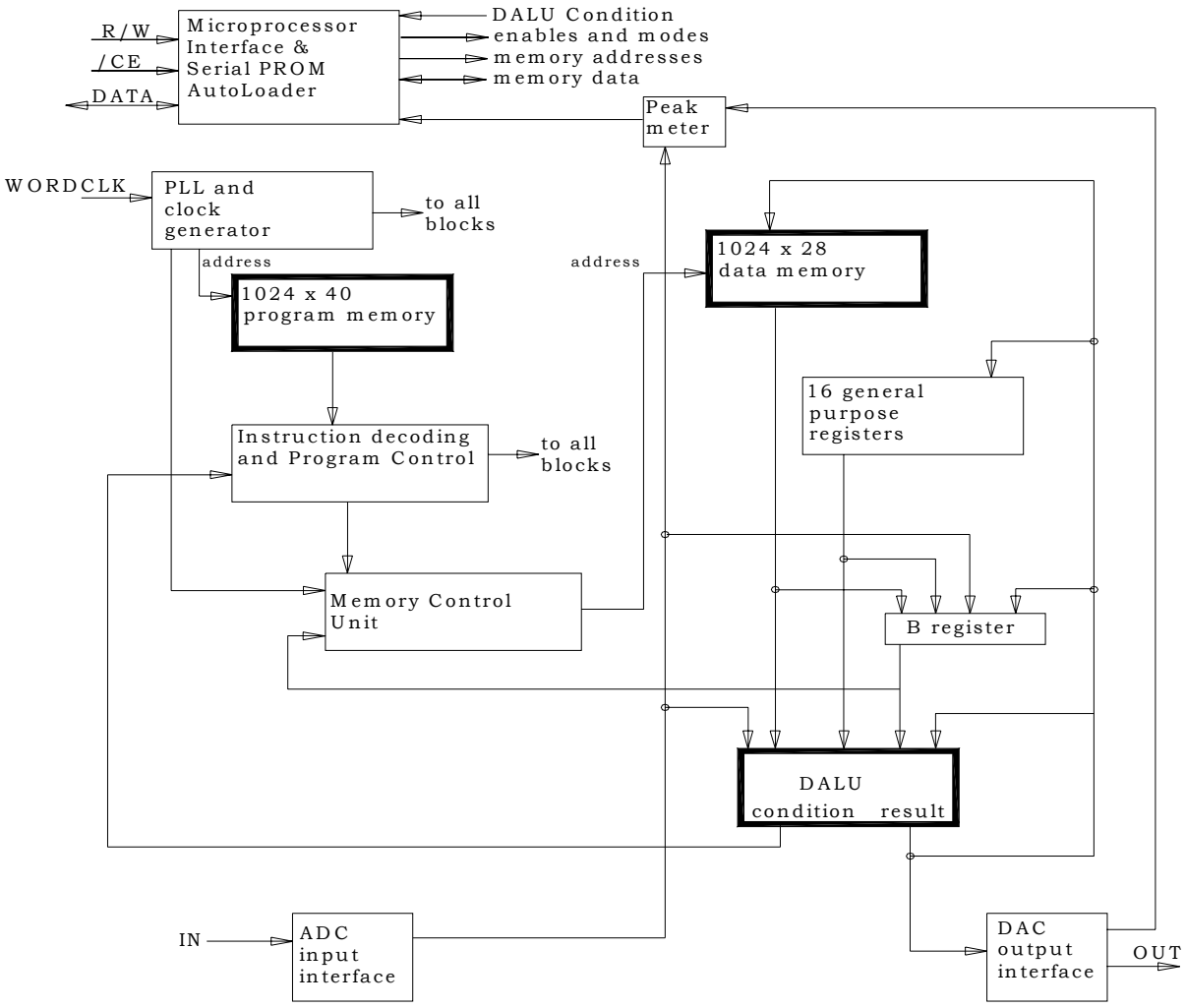
Note 1: If V_{DD} will always be below 3.6V (including the effects of ripple, spikes, etc.) then V_{DD} should be connected to BYPASS.

Note 2: Tested using AN310106.ASM which uses the AL3101 to its fullest.

Core Architecture

The DSP-1K contains the following blocks:

- Data/arithmetic/logic unit (DALU)
- 16 28-bit general purpose registers
- 1K x 40-bit program memory
- 1K x 28-bit data memory
- Memory control unit
- ADC input interface
- DAC output interface
- Instruction decoding and program control unit
- PLL and clock generator
- Microprocessor interface
- Serial PROM auto-loader
- Peak-metering unit
- Miscellaneous blocks



ARCHITECTURE OVERVIEW

Data/Arithmetic/Logic Unit

The DALU performs all the arithmetic and logical operations on the data in the DSP-1K. All instructions are executed in one clock cycle. The DALU is a fixed-point unit using a sign-integer-fraction format. In general, this format is S3.X where 'S' indicates the sign bit, '3' is the number of integer bits and 'X' is the number of fractional bits. 'X' will depend on the instruction being executed. If the instruction uses less than the number of available bits then the most significant bits are used. If the instruction uses more than the number of available bits then the number is 0 padded in its LSBs. The DALU consists of:

- A 28-bit x 22-bit multiplier producing a 28-bit result. The 28-bit number is in a S3.24 (sign bit, 3 integer bits and 24 fractional bits) and the 22-bit number is in a S3.18 format.
- a 28-bit accumulator in S3.24 format
- a 28-bit register (B) in S3.24 format that the accumulator may be copied to
- 16 28-bit general purpose registers in S3.24 format
- ADC input registers
- DAC output registers

Program Memory
The program memory is continuously cycled through the 1024 instructions. The instruction execution is synchronized with the ADC inputs and DAC outputs such that a new sample is received after instruction 1023 is executed and before instruction 0 is executed.

Data Memory
Data memory is in the S3.24 format. The data memory is mapped in the range of 0 - $3FF of the internal memory map.

Memory Control Unit
To automatically implement circular addressing, the effective address of a memory location is calculated by adding the address portion of the instruction to a counter that decrements once each sample period. (This offset is not added to the addresses which access the ADC input, DAC output or the 16 general purpose registers.) This counter is synchronized with the ADC inputs, DAC outputs and program counter such that it decrements after execution of instruction 1023 and before execution of instruction 0. This feature may be turned off if desired (Control Word 1 bit 1).

ADC Input Interface
ADC and DAC data rates are 64 times the WORDCLK frequency. ADC data is read into the 24 LSB's and sign extended into the integer and sign bits to create a 28-bit number. This results in the ADC having an effective range of +0.5 to -0.5. As an example, a full scale negative 24-bit ADC input of $800000 would become $F800000, which in the S3.24 format is equivalent to -0.5. The ADC inputs are read from addresses $410 - $417.

It is also possible to directly read the input pins IN0 - IN3 (pins 2-5). Reading address $419 will read IN3 - IN0 into bits 23-20 (just below the binary point). This allows the user to use these pins as flags within a program.

DAC Output Interface
DAC outputs are taken as the 24-LSB's of the number written to them. This aligns the DAC out with the ADC in. The MSB's are checked to verify they are all the same as the sign bit. If not, the value is limited as maximum negative or positive depending on the sign bit prior to being written to the DAC register. The DAC outputs are written to addresses $410 - $417. Though these addresses are the same as for the ADC, they are separate registers and will not overwrite the ADC values.

It is also possible to directly drive the serial output pins OUT0 - OUT3. By writing to the range $421-$42F, bits 23-20 of the data can be placed on the pins. Which pins are written to are controlled by the 4 LSB's of the address. If bit 0 of the address is set (i.e. address $421), OUT0 will reflect the data from bit 20, the remaining outputs will operate in the normal serial output mode. If bits 1 and 2 of the address were set (i.e. address $426), OUT1 would reflect data from bit 21 and OUT2 would reflect data from bit 22, OUT0 and OUT3 would continue to operate in their current mode. Once a pin is directly written to, it will stay in this direct write mode until it is written to as a serial output by writing to the range $410-$417.

Addr.	Outputs	Bits
$421	OUT0	20
$422	OUT1	21
$423	OUT1, OUT0	21,20
$424	OUT2	22
$425	OUT2, OUT0	22,20
$426	OUT2, OUT1	22,21
$427	OUT2, OUT1, OUT0	22,21,20
$428	OUT3	23
$429	OUT3, OUT0	23,20
$42A	OUT3, OUT1	23,21
$42B	OUT3, OUT1, OUT0	23,21,20
$42C	OUT3, OUT2	23,22
$42D	OUT3, OUT2, OUT0	23,22,20
$42E	OUT3, OUT2, OUT1	23,22,21
$42F	ALL	23-20

Serial PROM Autoloader (1KM Only)

If the AUTO pin (pin 6) is low at power on, the serial PROM autoloader is enabled and the 1KM loads its program information from the serial PROM. The SERIALM pin (pin 8) must be high.

Choosing the Microprocessor Interface (1KM Only)

The DSP-1KS uses only the serial micro interface. The 1KM provides for either parallel or serial interfaces, depending on the state of the SERIALM pin (pin 8). If SERIALM is low, the 1KM uses the serial microprocessor interface as described in **Serial Micro Interface**. If high, the 1KM uses the parallel microprocessor interface. In either case, the AUTO pin (pin 6) must be high.

Function	Pin 6	Pin 8
Reserved	0	0
Autoload – serial EEPROM	0	1
Serial µP interface	1	0
Parallel µP Interface	1	1

PLL and Clock Generator

The built-in PLL generates all necessary clocks from WORDCLK. This minimizes the external component count and lowers interconnection bandwidth, reducing EMI.

Peak-Metering Unit

Each sample period the peak-metering unit tests the 16 most significant bits of the serial inputs and outputs, and saves the highest peak absolute value since the last reading of the meter.

The scale of the reading approximates a logarithm. The scale is 2 units per decibel with a maximum value of $FC. The following table shows the relationship between the ADC or DAC absolute value and the peak meter result returned. Very small values deviate from a true log (as shown below), but above $000008 the log conformance is good.

ADC/DAC Value	Peak meter result
$000000	$00
$000001	$02
$000002	$04
$000003	$05
$000004	$07
$000005	$08
$000006	$09
$000007	$0B
$000008	$0C
.....	...
$000010	$18
.....	...
$6BFFFF	$F8
$75FFFF	$F9
$7FFE00	$FB
$7FFF00	$FC

When a meter is read, it is automatically cleared so that new peak values can be accumulated.

The result $FC is a special value indicating that the value being read is the largest possible number that can be expressed in 16 bits. You may consider it an indication that the number in question is either clipped or on the verge of clipping.

The peak meter circuit approximates absolute value by taking the ones complement of negative numbers. From that absolute value, shifting and table lookup determine the reading. The following table illustrates the results for very small and very large inputs. In the range $000020 to $7FFEFF the peak meter reading is determined exactly by calculating the sum $24 + (12*S) + L. S is the number of bits that the leading one is further left than $000020. (For example, S is 5 for $000400.) L is the value from the table lookup, which is indexed by the 5 bits to the right of the leading one.

Lower limit	Upper limit	Result L
00000	00001	$0
00010	00011	$1
00100	00101	$2
00110	00111	$3
01000	01010	$4
01011	01100	$5
01101	01111	$6
10000	10010	$7
10011	10101	$8
10110	11000	$9
11001	11011	$A
11100	11111	$B

MEMORY MAPS

Parallel Microprocessor Interface Memory Map (1KM Only)

The 1KM allows read and write access to the internal instruction RAM, sample memory and general purpose registers. In addition, there are peak meters on all 8 input and output channels that may be read, control registers that may be written to and a status register that may be read. Selection of the data to be read or written is done through a combination of address and settings in the control words.

Reads

Address			
A2	**A1**	**A0**	**Description**
0	0	0	Data LSB (Least Significant Byte)
0	0	1	Data
0	1	0	Data
0	1	1	Data
1	0	0	Data MSB (Most Significant Byte)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Status Word

Writes

Address			
A2	**A1**	**A0**	**Description**
0	0	0	Data LSB (Least Significant Byte)
0	0	1	Data
0	1	0	Data
0	1	1	Data
1	0	0	Data MSB (Most Significant Byte)
1	0	1	Target address LSB
1	1	0	Target address MSB (see "Note on Address MSB")
1	1	1	Control Words

Note on Address MSB

In RAM access mode, the format of "Address MSB" is:

Bit #	Description
0	Address bit 8
1	Address bit 9
3,2	Select RAM to write to: 00: Instruction RAM, 01:Reserved, 10: Sample RAM, 11:Direct access memory and serial I/O
4	0: Execute a write, 1: Execute a read
5	0: Execute access on instruction 1023, 1: Execute access immediately. NOTE: An immediate access to sample RAM or serial I/O can corrupt the memory if the DSP-1K is executing an access to memory at the same time. The safest way to do this is to make instruction 1023 an instruction that does no access to memory or any of the serial I/O and set this bit to 0. If immediate access is required, then the external device accessing the DSP-1K should monitor the WORDCLK signal. The device can then determine the instruction being executed and determine if it is safe to access the memory. Writes (but not reads) to general purpose registers are also subject to this restriction.
6	Test, always write 1
7	Always write 1

When the Target address MSB is written to address 6, the data written to addresses 0-4 is written to the target address. Note that Target address MSB has bits in it that define which internal memory is being written to/read from, the style, etc.

Control Words

Both control words are at address 7. Bit 7 indicates which control word is being written.

Control Word 0

Bit #	Description
0	ADC/DAC select (0 default) see next table
1	ADC/DAC select (0 default) see next table
2	0: Mute serial inputs,1: Enable serial inputs (0 default)
3	0: Mute OUT0, 1: Enable OUT0 (0 default)
4	0: Mute OUT1, 1: Enable OUT1 (0 default)
5	0: Mute OUT2, 1: Enable OUT2 (0 default)
6	0: Mute OUT3, 1: Enable OUT3 (0 default)
7	0: selects control word 0

ADC/DAC select in Control Word 0, bits 1-0

Bits1:0	Description
0	16 bit, ADC left justified, DAC right justified
1	20 bit, ADC left justified, DAC right justified
2	20 bit, ADC and DAC left justified
3	24 bit, ADC and DAC left justified

Control Word 1

Bit #	Description
0	Reserved, always write 0 (0 default)
1	0: Enable, 1: Disable memory offset counter (1 default)
2	0: Truncate MAC results, 1: Round MAC results (0 default)
3	0: Normal word clock, 1: Invert word clock (0 default)
4	0: Read input peak meters, 1: Read output peak meters (0 default)
5	0: Read peaks, 1: Read status and ram (0 default)
6	0: Enable, 1: Disable writing to memory under program control (1 default)
7	1: selects control word 1

Status Word

Bit #	Description
0	1: Memory access pending, 0: Memory access complete
1	1: Inputs are muted
2	1: OUT0 is muted
3	1: OUT1 is muted
4	1: OUT2 is muted
5	1: OUT3 is muted
6	1: An overflow occurred in the MAC
7	1: An overflow occurred in the DAC outs and output was clipped

MAC overflows are clipped except on integer instructions

Instruction/RAM/Status register access

To enable reading from this area, set bit 5 of control word 1 to "1". Writes may be done independent of the setting of that bit. All data is LSB aligned. Note that "Data" reads and writes use 5 bytes to contain all 40 bits of an instruction word. When non-instruction "Data" words are accessed, only 28 bits are used, so all of address 100 and the upper half of address 011 are zero.

Peak Reading: Input

To set this mode to read peak registers set bit 5 of control word 1 to "0" and set bit 4 of control word 1 to "0".

Reads

Address			
A2	**A1**	**A0**	**Description**
0	0	0	Read channel 0 input peak register
0	0	1	Read channel 1 input peak register
0	1	0	Read channel 2 input peak register
0	1	1	Read channel 3 input peak register
1	0	0	Read channel 4 input peak register
1	0	1	Read channel 5 input peak register
1	1	0	Read channel 6 input peak register
1	1	1	Read channel 7 input peak register

Peak Reading: Output

To set this mode to read output peak registers set bit 5 of control word 1 to "0" and set bit 4 of control word 1 to "1".

Reads

Address			
A2	**A1**	**A0**	**Description**
0	0	0	Read channel 0 output peak register
0	0	1	Read channel 1 output peak register
0	1	0	Read channel 2 output peak register
0	1	1	Read channel 3 output peak register
1	0	0	Read channel 4 output peak register
1	0	1	Read channel 5 output peak register
1	1	0	Read channel 6 output peak register
1	1	1	Read channel 7 output peak register

Serial Microprocessor Interface Memory Map (1KM and 1KS)

Writes

Address	Description
000H – 3FFH	Instruction RAM
400H	Control Word 0
401H	Control Word 1
800H – BFFH	Data RAM
C00H – C0FH	General purpose registers

Reads

Address	Description
000H – 3FFH	Instruction RAM
407H	Status register
500H – 50FH	Peak registers
800H – BFFH	Data RAM
C00H – C0FH	General purpose registers

Internal Program Memory Map

Address	Description
$0 - $3FF	Sample (Data) memory
$400 - $40F	Direct access memory
$410 - $417	Serial I/O
$418	LOG16 field extract – READ ONLY
$419	Direct input – READ ONLY
$41B	Null output – WRITE ONLY
$421 - $42F	Direct output – WRITE ONLY

Addresses in the range of $0 - $3FF are calculated by taking the address and adding it to a counter that is auto-decremented every sample period.

Addresses in the range $400 and up are not added to the address counter.

Reads from addresses $410 - $417 read the serial inputs, writes write to the serial outputs.

Methods of controlling the DSP-1K

The DSP-1KM has 3 interface methods by which external devices may control it. The 1KS only supports the serial micro interface.

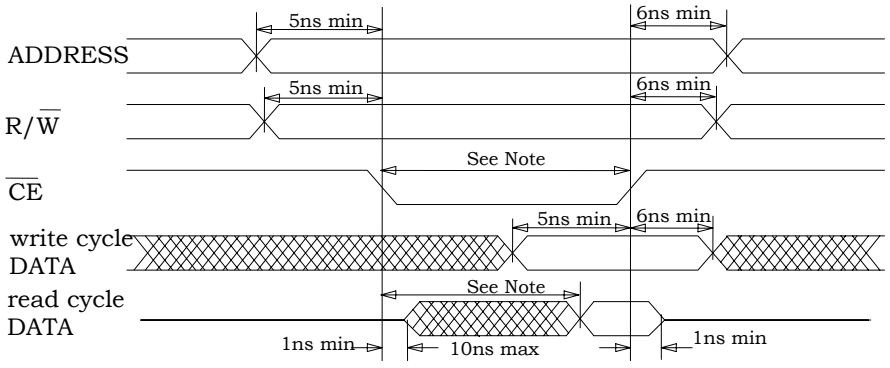
Parallel interface: Standard 8-bit micro interface. To select this interface, set pins 6 and 8 high. See **"Parallel Micro Interface"** for an explanation. Not available in 1KS.

Serial micro interface: the host micro communicates to the DSP-1K in a special serial format. To select this interface, set pin 6 high and pin 8 low. See "**Serial Micro Interface**" for an explanation of the format. 1KS uses this method only.

Auto load interface: In this mode, the 1KM will operate without a host micro and on power-up automatically load its code from a serial EEPROM. To select this mode, set pins 6 low and 8 high. See section **"Autoload Interface"** for an explanation of the format. This method is not available in the 1KS.

Parallel Micro Interface

The parallel micro interface is conventional. The R/W and address pins must be set up before the CE pin pulses low, and held until after CE is high again. During writes (R/W low) data must be stable around the rising edge of CE. During reads, data becomes stable shortly after CE falls and remains valid until shortly after CE rises.



Note: CE width min = read cycle DATA valid after CE falls max = (WORDCLK cycle/1024 + 32 ns)
(52 ns @ 48kHz WORDCLK)

Serial Micro Interface

Memory Map

Write

Address	Description
000H – 3FFH	Instruction RAM
400H	Control Word 0
401H	Control Word 1
800H – BFFH	Data RAM
C00H – C0FH	General purpose registers

Read

Address	Description
000H – 3FFH	Instruction RAM
407H	Status register
500H – 50FH	Peak registers
800H – BFFH	Data RAM
C00H – C0FH	General purpose registers

Control Word 1 differs from the Parallel Micro Interface by having one more bit. Bit 7 controls the Immediate/Last data access function. Set to one, accesses are immediate (not recommended). Set to zero, accesses are delayed until the last instruction execution time. Bits 4 and 5, which with the parallel interface control access to peak metering, have no effect with the serial interface.

The “Last” data access function is required for reads and writes to the data ram and writes to the general purpose registers.

When using the “Last” data access function for reads, the microprocessor driving the DSP-1K must pause after sending the last address bit clock. Clocking to receive the data read must not resume until after instruction 1023 is executed. This delay may be achieved by waiting one full sample period, or waiting until the DSP-1K’s internal word clock rises. (If Control Word 1 bit 3 is low, the internal word clock follows the external WORDCLK. If the bit is high, the internal word clock is the inversion of the external WORDCLK.)

The reason for using the “Last” data access function is that the microprocessor data memory read/write function shares timing with the internal use of the data memory. If access is immediate and unsynchronized, it may coincide with data access by the DSP-1K’s own program, resulting in corrupted data. By using the “Last” function, and making sure that instruction 1023 does not read or write data memory, the access occurs during instruction 1023 without disturbing the DSP-1K’s processing.

Serial Micro Interface Format and Timing

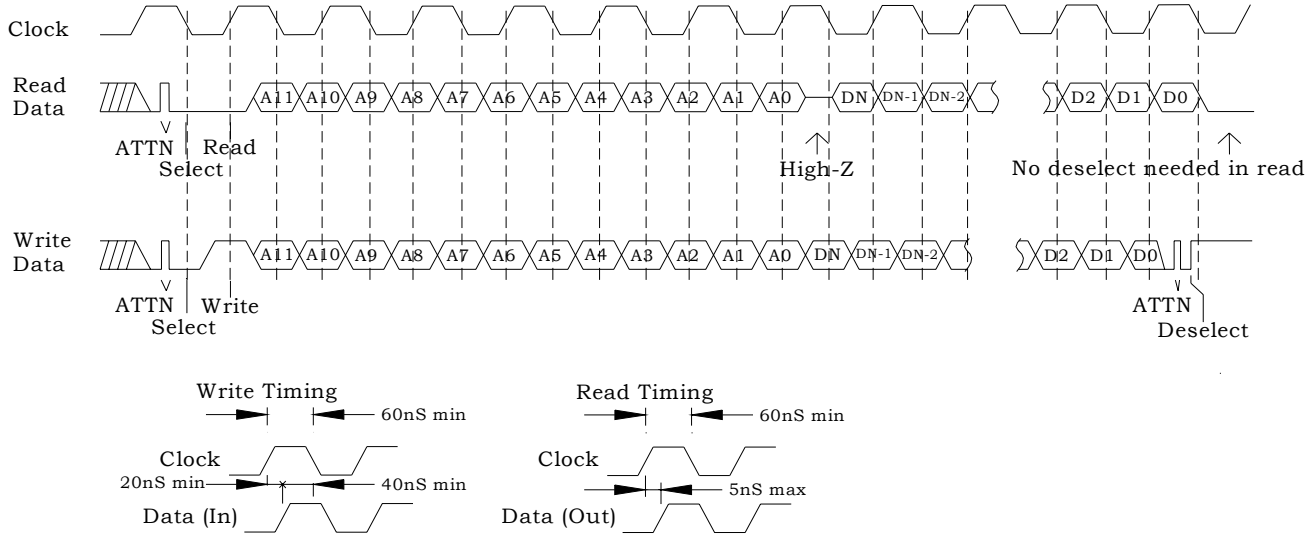
Format for serial interface:
ATTN SEL* R*/W A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 DN DN-1 DN-2 ... D2 D1 D0 ATTN DESEL

In write mode only

ATTN: A low to high to low is used as attention or start signal
Sel: 0=Select, 1=Deselect
R*/W: 0=Read, 1=Write
A11 - A0: Address
D7 - D0: Data

Notes:

1. There is a period of High-Z during a read between A0 and first data bit shifted out. When the "Last" function is in use, the clock for the first data bit must be delayed until after instruction 1023.
2. As long as data is being sent during a write, the address will be automatically incremented so only a start address need be sent.
3. Clock phase is not important.



Autoload Interface

Program information and control words can be loaded from a serial "configuration EEPROM" such as the ATMEL AT17C65. A capacity of 1024 words x 5 bytes + 2 control bytes = 5122 bytes or 40976 bits is required. The first bit from the EEPROM is the most significant bit of the first instruction (program address 0) of the 1KM. The second bit from the EEPROM is the 2nd most significant bit of the first instruction word, and so forth. The 41st bit from the EEPROM is the MS bit of the second instruction of the 1KM. This pattern continues until 40960 bits are used, the 40960th bit is the least significant bit of the last word in the 1KM's instruction memory. The next 8 bits fill Control Word 0 of the 1KM, most significant bit first; the following 8 bits fill Control Word 1. Any other bits in the EEPROM are ignored.

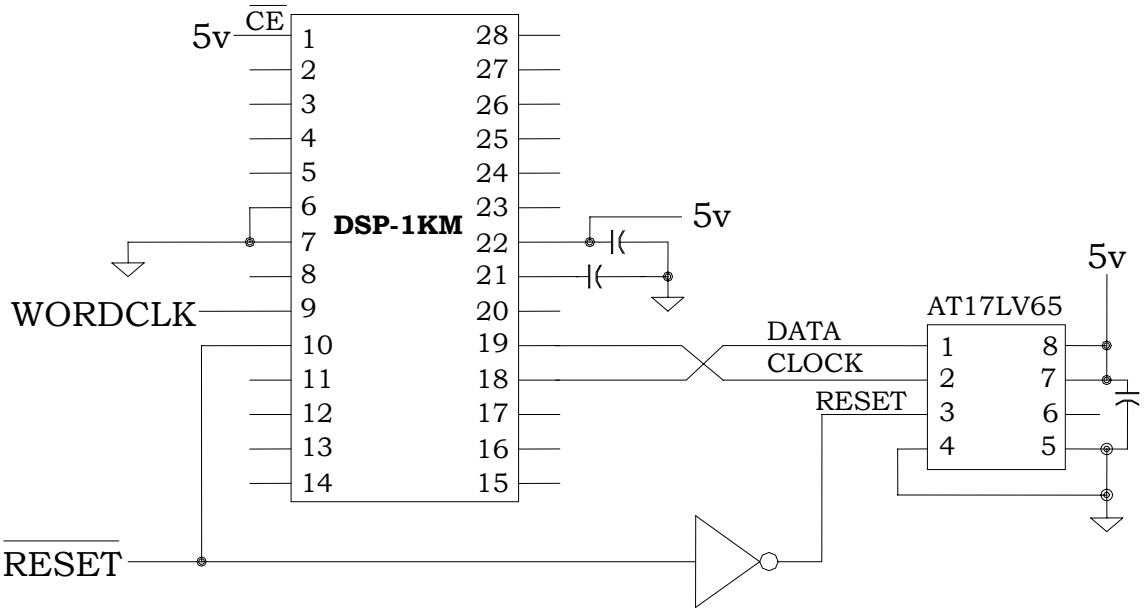
Order of events during autoload

The /AUTO and /RST pins must be held low while power supplies stabilize; /SERIALM must be high. After circuits external to the 1KM drive /RST high, the 1KM waits 1024 WORDCLK periods. For each of the next 1024 WORDCLK periods, the 1KM produces forty 160 ns pulses spaced 160 ns apart (320 ns period) on pin 19 (D1). At each rising edge one bit is accepted on

pin 18 (D0). The first forty pulses load instruction address 0, the next forty instruction address 1, and so forth. The MSB is loaded first.

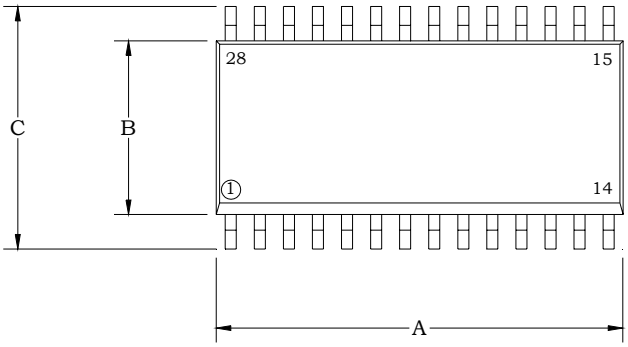
Sixteen more pulses are produced, loading Control Word 0 and Control Word 1, both MSB first.

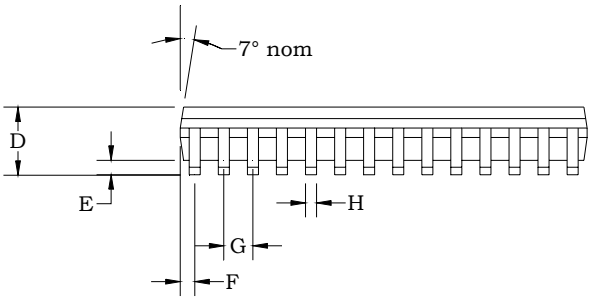
The loaded program runs for 1024 WORDCLK periods with Serial I/O muted, then Serial I/O is unmuted (if control bits allow).

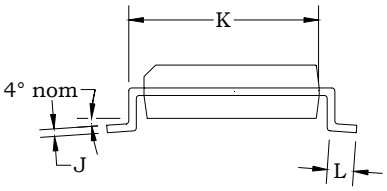


Package Dimensions

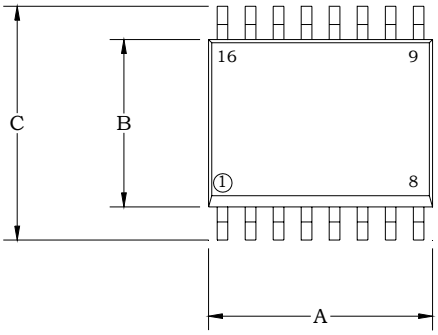
AL3101 - 28-pin

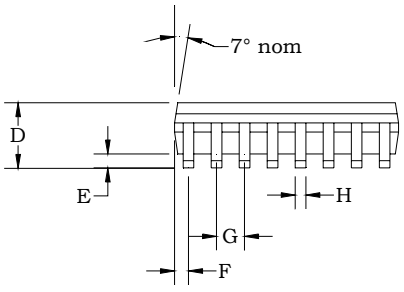


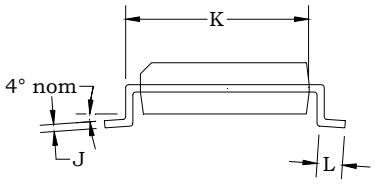




	Dimensions (Typ)	
	Inches	Millimeters
A	0.705"	17.90
B	0.297"	7.54
C	0.406"	10.32
D	0.090"	2.28
E	0.008"	0.02
F	0.030"	0.76
G	0.050"	1.27
H	0.017"	0.40
J	0.011"	0.27
K	0.329"	8.33
L	0.033"	0.83







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