dream SAM3416

# HIGH PERFORMANCE AUDIO DSP WITH USB

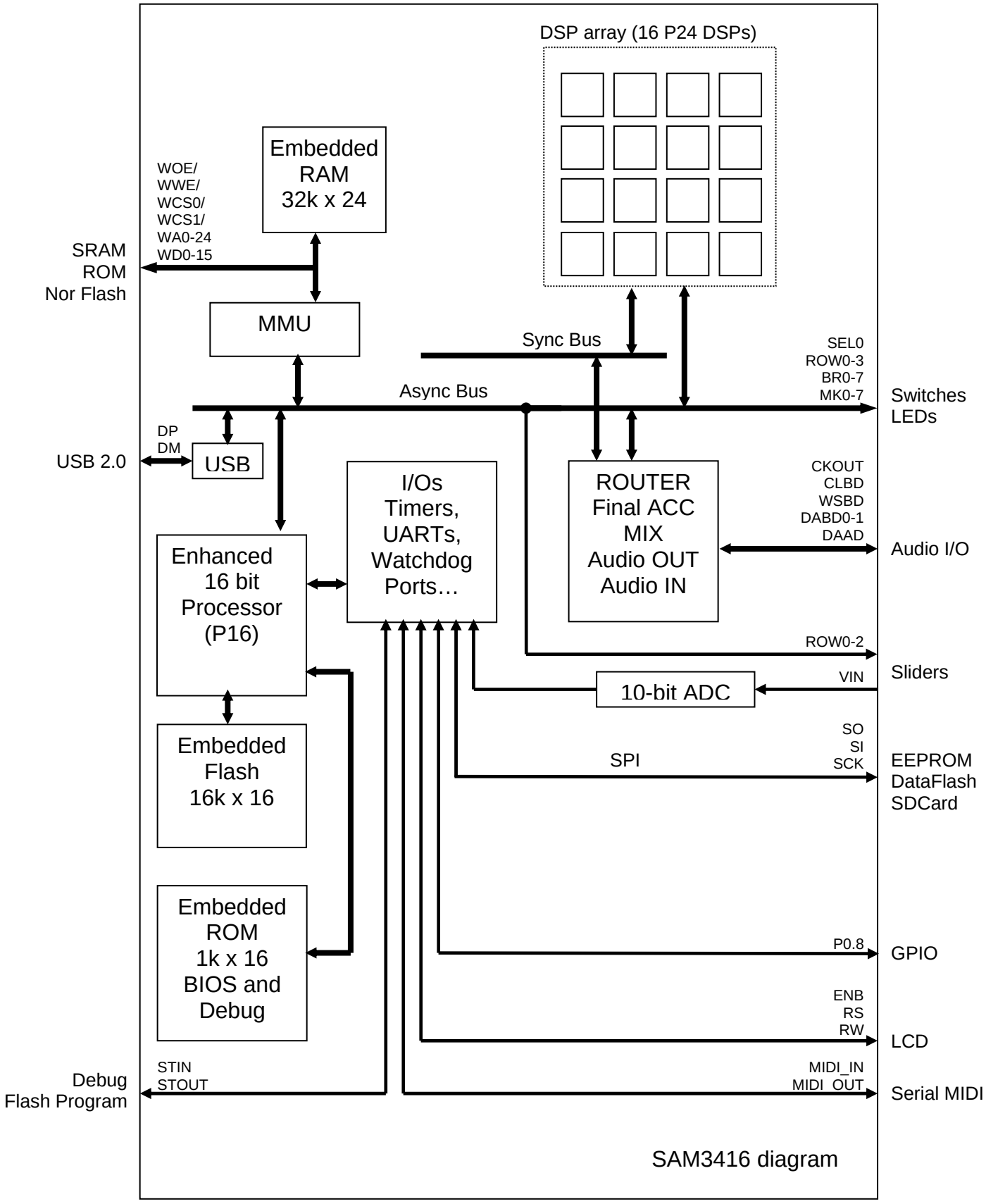
## Key features

- professional Effects: Reverb, Chorus, Compressor, Distortion, Equalizer, etc
- USB 2.0 (full-speed) interface for AudioClass 1.0 compliant Audio/MIDI I/F
- Audio Player: MP3, WAV, MIDI
- up to 126 voices high quality Sound Synthesis
- external memory up to 2 x 64 MBytes
- various high quality sound sets available
- direct connection to Switches, LEDs, Potentiometers & Sliders
- 8-bit parallel LCD port
- 2 channels digital Audio IN, 4 channels digital Audio OUT (24bit)
- serial MIDI IN/OUT
- SPI (mode 0) interface for DataFlash®, EEPROM, or SD-Card
- up to 42 General Purpose I/O pin
- 16 24bit DSP's with double precision instructions and enhanced Audio routing
- P16 Microcontroller with optimized instruction set for C compiler
- Built-in RAM 32k x 24 for Effects delay lines etc.
- Built-in Flash 16k x 16 for resident firmware and code protection
- Fuse bits for Configuration and Security
- Watchdog
- deep Power Down
- 128-pin LQFP package

## Typical applications

- High Quality Multi-Effects with USB
- Highly integrated digital Guitar Amp with Audio Player and USB
- High Performance Electronic Drum Sound module

## 1. SAM3416 Internal Architecture



The SAM3416 is a member of the SAM3000 family of sound synthesis/processing ICs that uses the DSP array technology.

The SAM3416 includes sixteen 24-bit DSPs, a 24-bit Audio Router and a general-purpose 16-bit processor with new instructions and a C compiler for quicker reliable firmware development.

The SAM3416 can handle up to 64 switches. Switches, organized in matrix form, require only a serial diode. Up to 64 LEDs can be directly controlled by the SAM3416 in a time multiplexed way. Additional LEDs can be connected through additional external shift registers using the GPIO lines (general purpose I/O) of the SAM3416. The built-in analog to digital converter of the SAM3416 allows connecting continuous controllers like sliders, potentiometers, control pedals etc.

The SAM3416 can be directly connected to most LCD displays through an 8-bit dedicated data bus and 3 control signals.

A variety of I/Os, including USB 2.0 Full Speed, Wave ROM, DataFlash® are provided. Sampling rates of 48KHz or 44.1KHz at 24 bits are supported.

**- DSP Array**

The SAM3416 includes 16 on-chip DSPs.
Each DSP (P24) is built around a 2k x 24 RAM and a 1.2k x 24 ROM. The RAM contains both data and P24 instructions; the ROM contains typical coefficients such as FFT cosines and windowing. A P24 sends and receives audio samples through the Sync Bus. It can request external data such as compressed audio through the Async Bus. Each P24 RAM can be accessed through the Async Bus.
Each P24 is capable of typical MAC operation loops, including auto-indexing, bit reverse and butterfly (multiplication of complex numbers). It also includes specialized audio instructions such as state variable IIR filtering, envelope generation, linear interpolation and wavetable loop. The DSP's have new 48-bit double precision instructions for improved Pro Audio applications.
One P24 is sufficient for processing one channel MPEG1 Layer2, implementing a multi-tap delay line or Reverb etc.

**- Sync Bus**

The Sync Bus transfers data on a frame basis, typical frame rates being 32, 44.1, 48, 96 kHz. Each frame is divided into 32 time slots. Each slot is divided into 8 bus cycles. Each P24 is assigned a hardwired time slot (16 to 31), during which it may provide 24-bit data to the bus (up to 8 data samples). Each P24 can read data on the bus at any time, allowing inter P24 communication at the current sampling rate. Slots 0 to 15 are reserved for a specific router DSP, which also handles audio out, audio in, and remix send.

**- Async Bus**

The Async Bus is 24-bit data inside the chip and 16-bit outside.
The P16 processor normally masters the Async Bus, it can read/write the P24 memories and the external ROM/RAM or embedded RAM. However, each P24 can request a bus master cycle for accessing external ROM/RAM or other P24 memories. This allows efficient intercommunication between several P24s on asynchronous block basis. Specific P24 instructions FLOAT and FIX allow to convert fixed point DSP data to floating point 16 bits. This allows for 20-bit audio dynamic range when using 16-bit external memory.

**- Enhanced 16-bit processor**

This is the enhanced version of P16 processor with added instructions allowing optimized use of C compiler. A built-in Flash is connected to the P16 to allow fast code fetch. The P16 ROM holds basic input/output software (BIOS) for peripherals such as UART, DataFlash®, as well as a debugger which uses a dedicated asynchronous serial line, or interface with host processor though a 8-bit parallel port. The firmware can reside on the built-in 16k x 16 Flash or it can be downloaded at power-up into the built-in 32k x 24 RAM from host.

**- MMU (memory management unit)**

The MMU handles transfer requests between the external memories (SRAM, NOR Flash, ROM) or embedded RAM, the P16 and the P24s through the Async Bus. The SAM3416 includes an on chip 32k x 24 RAM.

**- Router: final ACC, MIX, audio out, audio in**

This block includes a RAM, accessed through the Async Bus, which defines the routing from the Sync Bus to/from the Audio I/O or back to the Sync Bus (mix send). It takes care of mix and accumulation from Sync Bus samples. 16 channels of audio in and 16 channels of audio out are provided (8 stereo in/out, I2S or MSB Left format). The stereo audio in channel may have a different sampling rate than the audio out channels. In this case, one or more P24s take care of sampling rate conversion.

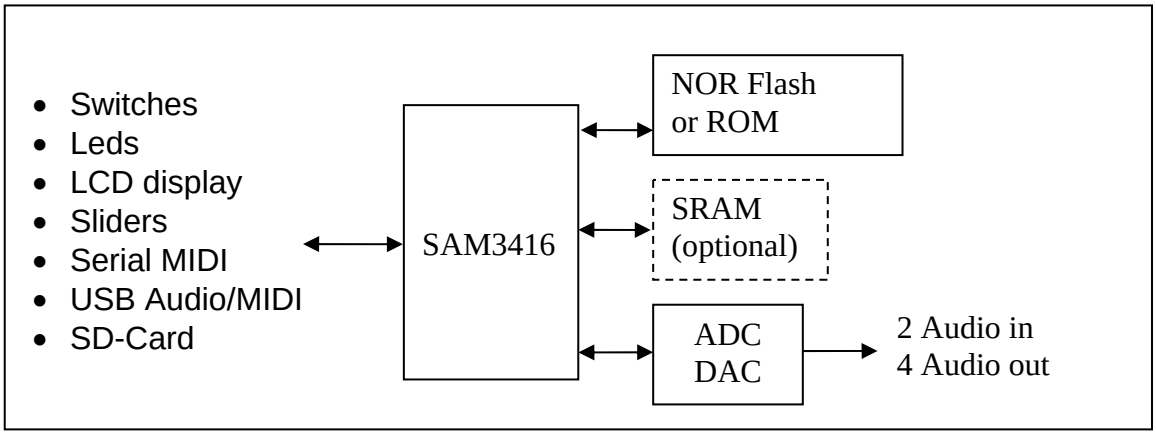
**- I/O**

The SAM3416 includes very versatile I/Os, that share common pins for reduced pin count and small IC footprint. Most I/Os, when not used for a specific function, remain available as firmware controlled general-purpose pins.
The following peripherals are included on chip:

- 2 x 8-bit timers
- 2 x 16-bit timers
- USB2.0 Full Speed
- 2 x asynchronous bi-directional serial port (one used as debug interface).
- Synchronous serial slave port (SPI type host connection).
- Synchronous serial master port (SPI type peripherals connection).
- Firmware controlled I/O pins, for connection to LCD display, switches, etc.

# 2. Typical application examples

## 2.1. Digital Guitar Amp / Multi-Effect with USB




- Direct connection to Switches, LEDs, LCD, …
- 10-bit ADC for Potentiometers and Sliders
- High quality Effects: Compressor, Distortion, Reverb, Modulation Effects, Delay etc.
- Direct connection to SD-Card for Audio file playback (MP3, WAV, MIDI)
- MIDI Synthesis with legendary Dream high quality wavetable sound
- USB 2.0 Full Speed

# 3. SAM3416 capacity and I/O configuration

The SAM3416 can run firmware directly from an embedded Flash memory or from an external ROM/Flash/SRAM memory. It may also run firmware from local RAM. The SAM3416 is the ideal choice for high range effects units with USB, external components low count and many I/O pins.

## 3.1. DSP considerations

The SAM3416 includes 16 x P24 DSPs.
The table below lists the performance achievable by the P24:

| Function | P24s required |
|---|---|
| MPEG1 Layer2 single track decode | 1 |
| MPEG1 Layer3 (MP3) decode (stereo) | 3 |
| 9-voice wavetable synthesis@48kHz | 1 |
| Stereo Reverb and Chorus @48kHz | 1 |
| Stereo 10-band equalizer @48kHz | 1 |
| Stereo 31-band equalizer @48kHz | 3 |

## 3.2. I/O selection considerations

I/Os are organized in groups, which can be mutually exclusive because they share the same IC pins (please refer to the pin-out to identify the exclusions). The two main types of operation are host controlled and stand-alone.

### 3.2.1. Stand-alone operation

Possible stand-alone modes are:
- Firmware into built in Flash memory
- Firmware into built in Flash memory plus firmware extension in external memory.

# 4. SAM3416 PINOUT

## 4.1. Pin description

Identical sharing number indicates multifunction pins.
Pd indicates pin with built-in pull-down resistor. (Pd) indicates that the pull-down can be disabled.
Pu indicates pin with built-in pull-up resistor. (Pu) indicates that the pull-down can be disabled.
5VT indicates a 5 volt tolerant Input or I/O pin.
MEM indicates a pad supplied by VM33.

| Pin name | Pin# | Type | Sharing | Description |
|---|---|---|---|---|
| GND | 5,15,34,44, 53,80,98, 110,113,121 | PWR | - | Digital ground. All these pins should be returned to a ground plane. |
| AGND | 105 | PWR | - | Analog ground for the ADC. Should be returned to a clean analog ground plane. |
| VD18 | 102 | PWR | - | Power for the 2 internal PLL, +1.8V nominal (1.8V ± 10 %). These pin can be connected to the output of the regulator OUTVC182 (pin 45). A 100nF decoupling capacitor should be connected between these pin and a close ground pin (98). |
| VD33 | 46,79,111 | PWR | - | +3.3V power for internal 3.3V to 1.8 V regulators, USB device and periphery. All these pins should be returned to nominal 3.3V. |
| VM | 1,14,26,39, 116, | PWR | - | Memory PAD Power +2.3V to +3.6V. All VM pins should be returned to 3.3V |
| VA33 | 107 | PWR | - | Analog power for the ADC, +3.3V nominal (3,3V ± 10 %). |
| OUTVC181, OUTVC182 | 112,45 | PWR | - | 3.3V to 1.8 V regulators output. The 2 built-in regulators give 1.8V for internal use (core supply). PLL supply pin VD18 could also be connected to OUTVC182. Decoupling capacitors 470pF in parallel with 2.2 or 4.7µF must be connected between each OUTVC18x pin and GND |
| VREF | 12 | In | - | VM/2 reference for memory pads. |
| DB0-DB7 | 77,76,75,74, 73,72,71,70 | I/O 5VT (Pd) | 1 | LCD bi-directional data bus. |
| P0.0-P0.7 | 77,76,75,74, 73,72,71,70 | I/O 5VT (Pd) | 1 | General purpose I/O can individually be programmed as input or output |
| ENB | 83 | Out | 2 | LCD Enable, active high |
| P0.11 | 83 | I/O 5VT (Pu) | 2 | General purpose I/O pin |
| RW | 81 | Out | 3 | LCD: Select Write (low) or Read (high). |
| P0.12 | 81 | I/O 5VT (Pu) | 3 | General purpose I/O pin |
| RS | 82 | Out | 4 | LCD: Select Instruction (low) or Data (high) |
| P0.13 | 82 | I/O 5VT (Pu) | 4 | General purpose I/O pin |
| MIDI_IN | 84 | In 5VT Pu | 5 | Serial MIDI in |
| P0.14 | 84 | In 5VT Pu | 5 | General purpose input pin |
| MIDI_OUT | 85 | Out | 6 | Serial MIDI out |
| P0.9 | 85 | I/O 5VT | 6 | General purpose I/O pin |

| | | | | |
|---|---|---|---|---|
| DABD0 | 91 | Out | | Stereo channel 0 of digital audio output, I2S or MSB format |
| DABD1 | 92 | Out | 7 | Stereo channel 1 of digital audio output, I2S or MSB format |
| P2.8 | 92 | I/O 5VT | 7 | General purpose I/O pin |
| DAAD | 93 | In 5VT (Pd) | 8 | Stereo audio data input, I2S or MSB format. |
| P2.0 | 93 | I/O 5VT | 8 | General purpose I/O pin |
| CLBD | 89 | Out | - | Audio bit clock for DABD1-0 and for DAAD. |
| WSBD | 90 | Out | - | Audio left/right channel select for DABD1-0 and DAAD |
| CKOUT | 88 | Out | - | External DAC/Codec master clock. Can be programmed to be 128xFs, 192xFs, 256xFs, 384xFs, 512xFs, Fs being the DAC/Codec sampling rate. |
| WA24 | 43 | Out MEM | 9 | External memory address bit, extension to 512 Mbits |
| XCS02/ | 43 | Out MEM | 9 | Programmable Extended chip select for 2nd memory device |
| P1.9 | 43 | I/O MEM | 9 | General purpose I/O pin |
| WA23 | 42 | Out MEM | 10 | External memory address bit, extension to 256 Mbits |
| P1.8 | 42 | I/O MEM | 10 | General purpose I/O pin |
| WA22 | 41 | Out MEM | 11 | External memory address bit, extension to 128 Mbits |
| P1.7 | 41 | I/O MEM | 11 | General purpose I/O pin |
| WA21 | 40 | Out MEM | 12 | External memory address bit, extension to 64 Mbits |
| P1.6 | 40 | I/O MEM | 12 | General purpose I/O pin |
| WA20 | 38 | Out MEM | 13 | External memory address bit, extension to 32 Mbits |
| P1.5 | 38 | I/O MEM | 13 | General purpose I/O pin |
| WA19 | 37 | Out MEM | 14 | External memory address bit, extension to 16 Mbits |
| P1.4 | 37 | I/O MEM | 14 | General purpose I/O pin |
| WA18 | 36 | Out MEM | 15 | External memory address bit, extension to 8 Mbits |
| FS1 | 36 | In MEM | 15 | Freq sense, sensed at power up. FS1\|FS0 allow firmware to know operating freq of chip as follows (optional):<br>00- 12 MHz 01- 9.6 MHz 10- 11.2896 MHz 11- 12.288 MHz |
| P1.3 | 36 | I/O MEM | 15 | General purpose I/O pin |
| WA17 | 35 | Out MEM | 16 | External memory address bit, extension to 4 Mbits |
| FS0 | 35 | In MEM | 16 | Freq sense, sensed at power up. Together with FS1, allows the firmware to know the operating freq of the chip (see FS1) |
| P1.2 | 35 | I/O MEM | 16 | General purpose I/O pin |
| WA15, WA16 | 32,33 | Out MEM | 17 | External memory address bits, extension to 1 and 2 Mbits |
| P1.0,P1.1 | 32,33 | I/O MEM | 17 | General purpose I/O pins |
| WA0-WA14 | 16-25,27-31 | Out MEM | - | External memory address bits, up to 512 kbits (32k x 16) |
| WD0-WD15 | 119,120, 122-128, 2-4,6-9 | I/O MEM | - | External memory data |
| WCS1/ | 118 | Out MEM | - | External memory chip select 1, active low. Pre-decode for an external RAM/Flash/ROM. |
| WCS0/ | 117 | Out MEM | 18 | External memory chip select 2, active low. Pre-decode for an external RAM/Flash/ROM. When using more than one memory device, Extended Chip Select XCS11, and XCS02 can be used instead of WCS0/ |
| XCS11/ | 117 | Out MEM | 18 | Programmable Extended chip select for 1st memory device. |
| WOE/ | 114 | Out MEM | - | External memory output enable, active low. |
| WWE/ | 115 | Out MEM | - | External memory write enable, active low. |
| DFSI | 10 | Out MEM | - | DataFlash serial input (to DataFlash) |
| DFSO | 11 | In MEM | - | DataFlash serial output (from DataFlash). This pin should be grounded or pulled-down if not used. |
| DFSCK | 13 | Out MEM | - | DataFlash data clock |

| | | | | |
|---|---|---|---|---|
| ROW 0-ROW2 | 48-50 | I/O 5VT | - | I/O pin, fully under firmware control.<br>In standard use, ROW signals select: switches/LEDs row and external slider analog multiplexer (4051) channel. Eight rows combined with eight BR/MK columns allow to control 64 switches, 64 LEDs and 8 sliders. |
| SEL0 | 52 | I/O 5VT | - | I/O pin, fully under firmware control. |
| BR0-BR7 | 54-61 | I/O 5VT | - | I/O pin, fully under firmware control. |
| MK0-MK7 | 62-69 | I/O 5VT | - | I/O pin, fully under firmware control. |
| X1, X2 | 99,100 | - | - | External crystal connection. Standard frequencies are 12 MHz, 9.6 MHz, 11.2896 MHz, 12.288 MHz. Max frequency is 12.5 MHz. An external clock (max. 1.8Vpp) can be connected to X1 using AC coupling (22pF). A built-in PLL multiplies the clock frequency by 4 or by 6 for internal use.<br>No external compensation capacitors are needed. |
| LFT | 101 | - | - | PLL decoupling RCR filter. |
| USB_X1, USB_X2 | 103,104 | - | - | 12 MHz external crystal connection for the USB embedded device.<br>Crystal on USB_X1-USB_X2 is optional when crystal connected to X1-X2 is 12MHz. In this case USB clock can be internally derived from main clock.<br>No external compensation capacitors are needed. |
| USB_DP | 109 | I/O | - | USB D+ connection (analog). |
| USB_DM | 108 | I/O | - | USB D- connection (analog). |
| RESET/ | 94 | In 5VT | - | Master reset Schmitt trigger input, active low. RESET/ should be held low during at least 10ms after power is applied. On the rising edge of RESET/, the chip enters an initialization routine, which may involve firmware download from a host. |
| STIN | 86 | In 5VT<br>Pd | - | Serial test input. This is a 57.6 kbauds asynchronous input used for firmware debugging. This pin is tested at power-up. The built-in debugger starts if STIN is found high. STIN has a built-in pull-down. It should be grounded or left open for normal operation. |
| STOUT | 87 | Out | 19 | Serial test output. 57.6 kbauds async output used for firmware debugging. |
| MIDI_OUT2 | 87 | Out | 19 | Additional serial MIDI out |
| P0.8 | 78 | I/O 5VT | - | General purpose I/O pin |
| VIN | 106 | In | - | Potentiometer/Slider analog input. Ranges from AGND to VA33. Should hold the ROW[0-3] slider voltage. Multiple sliders should be connected through external analog multiplexer(s) like 4051. |
| PDWN/ | 96 | In<br>Pu | - | Power down, active low. When power down is active, WCS0/, WCS1/, WWE/, WOE/, MIDI_OUT, STOUT are output 1. Address and data lines are output 0. All other outputs are set to 0. The crystal oscillator is stopped and supply voltage is removed from the core. To exit from power down, PDWN/ must be set to VD33, then RESET/ applied. When unused this pin must be left open or connected to VD33. |
| TEST0, TEST1 | 95,97 | In<br>Pd | - | Test inputs. Should be grounded or left open. |
| TEST2, TEST3 | 47,51 | I/O 5VT | | Test I/O. Should be connected to ground through a 100k serial resistor. |

## 4.2. Alternate functions quick view

### 4.2.1. Functions per pin

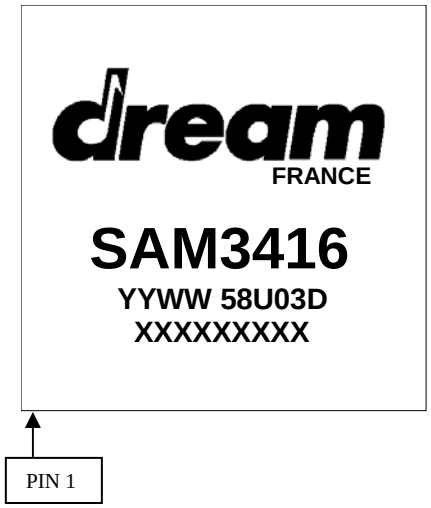
| Pin Name<br>Main Function | Alternate<br>Function 1 | Alternate<br>Function 2 | Alternate<br>Function 3 |
|---|---|---|---|
| | | | |
| **DEVICE INTERFACE** | | | |
| USB_DP – USB_DM | | | |
| DFSO | | | |
| DFSI | | | |
| DFSCK | | | |
| STIN | | | |
| STOUT | MIDI_OUT2 | | |
| MIDI_IN | | | P0.14 |
| MIDI_OUT | | | P0.9 |
| ENB | | | P0.11 |
| RS | | | P0.13 |
| RW | | | P0.12 |
| DB7 - DB0 | | | P0.7 - P0.0 |
| | | | P0.8 |
| **MEMORY INTERFACE** | | | |
| WCS0/ | | XCS11/ | |
| WCS1/ | | | |
| WOE/ | | | |
| WWE/ | | | |
| WD15 – WD0 | | | P4.15 - P4.0 |
| WA14 – WA0 | | | |
| WA16 – WA15 | | | P1.1 – P1.0 |
| WA17 | FS0 | | P1.2 |
| WA18 | FS1 | | P1.3 |
| WA19 | | | P1.4 |
| WA20 | | | P1.5 |
| WA21 | | | P1.6 |
| WA22 | | | P1.7 |
| WA23 | | | P1.8 |
| WA24 | | XCS02/ | P1.9 |
| **DIGITAL AUDIO IN/OUT** | | | |
| CKOUT | | | |
| CLBD | | | |
| WSBD | | | |
| DABD0 | | | |
| DABD1 | | | P2.8 |
| DAAD | | | P2.0 |
| **SWITCH/LED SCANNING** | | | |
| SEL 0 | | | |
| ROW2 – ROW0 | | | |
| BR7 – BR0 | | | |
| MK7 – MK0 | | | |
| VIN | | | |

## 4.3. Pin-out by pin #

| Pin# | Name | Pin# | Name | Pin# | Name | Pin# | Name |
|---|---|---|---|---|---|---|---|
| **1** | **VM** | **33** | WA16 | **65** | MK3 | **97** | TEST1 |
| **2** | WD9 | **34** | **GND** | **66** | MK4 | **98** | **GND** |
| **3** | WD10 | **35** | WA17 | **67** | MK5 | **99** | X1 |
| **4** | WD11 | **36** | WA18 | **68** | MK6 | **100** | X2 |
| **5** | **GND** | **37** | WA19 | **69** | MK7 | **101** | LFT |
| **6** | WD12 | **38** | WA20 | **70** | DB7 | **102** | **VD18** |
| **7** | WD13 | **39** | **VM** | **71** | DB6 | **103** | USB_X1 |
| **8** | WD14 | **40** | WA21 | **72** | DB5 | **104** | USB_X2 |
| **9** | WD15 | **41** | WA22 | **73** | DB4 | **105** | **AGND** |
| **10** | DFSI | **42** | WA23 | **74** | DB3 | **106** | VIN |
| **11** | DFSO | **43** | WA24 | **75** | DB2 | **107** | **VA33** |
| **12** | VREF | **44** | **GND** | **76** | DB1 | **108** | USB_DM |
| **13** | DFSCK | **45** | OUTVC182 | **77** | DB0 | **109** | USB_DP |
| **14** | **VM** | **46** | **VD33** | **78** | P0.8 | **110** | **GND** |
| **15** | **GND** | **47** | TEST2 | **79** | **VD33** | **111** | **VD33** |
| **16** | WA0 | **48** | ROW0 | **80** | **GND** | **112** | OUTVC181 |
| **17** | WA1 | **49** | ROW1 | **81** | RW | **113** | **GND** |
| **18** | WA2 | **50** | ROW2 | **82** | RS | **114** | WOE/ |
| **19** | WA3 | **51** | TEST3 | **83** | ENB | **115** | WWE/ |
| **20** | WA4 | **52** | SEL0 | **84** | MIDI_IN | **116** | **VM** |
| **21** | WA5 | **53** | **GND** | **85** | MIDI_OUT | **117** | WCS0/ |
| **22** | WA6 | **54** | BR0 | **86** | STIN | **118** | WCS1/ |
| **23** | WA7 | **55** | BR1 | **87** | STOUT | **119** | WD0 |
| **24** | WA8 | **56** | BR2 | **88** | CKOUT | **120** | WD1 |
| **25** | WA9 | **57** | BR3 | **89** | CLBD | **121** | **GND** |
| **26** | **VM** | **58** | BR4 | **90** | WSBD | **122** | WD2 |
| **27** | WA10 | **59** | BR5 | **91** | DABD0 | **123** | WD3 |
| **28** | WA11 | **60** | BR6 | **92** | DABD1 | **124** | WD4 |
| **29** | WA12 | **61** | BR7 | **93** | DAAD | **125** | WD5 |
| **30** | WA13 | **62** | MK0 | **94** | RESET/ | **126** | WD6 |
| **31** | WA14 | **63** | MK1 | **95** | TEST0 | **127** | WD7 |
| **32** | WA15 | **64** | MK2 | **96** | PDWN/ | **128** | WD8 |

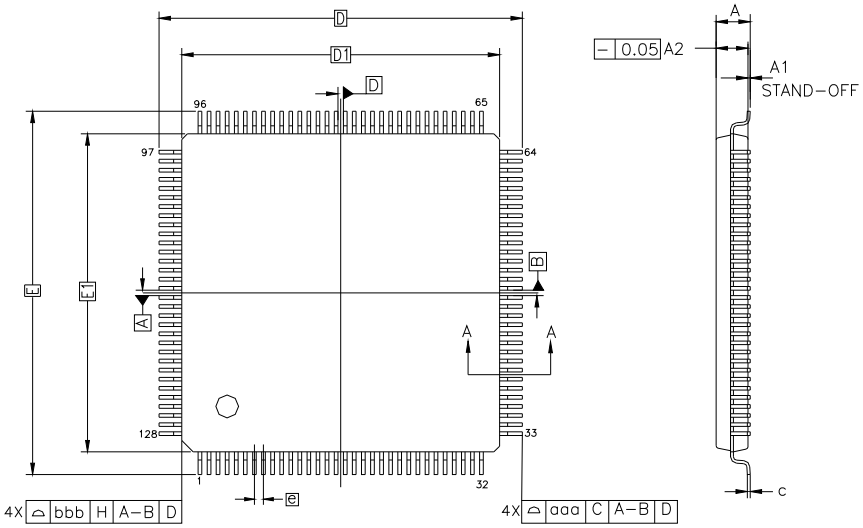
## 5. Marking

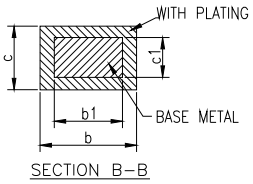
R-LQ128_G



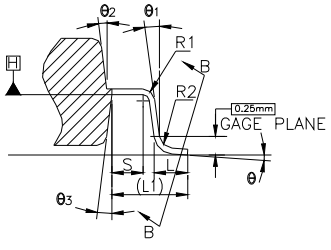
# 6. Mechanical dimensions

**R-LQ128_G - LQFP**




SECTION B–B




SECTION A–A

ALL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BASIC | | | 0.630 BASIC | | |
| D1 | 14.00 BASIC | | | 0.552 BASIC | | |
| E | 16.00 BASIC | | | 0.630 BASIC | | |
| E1 | 14.00 BASIC | | | 0.552 BASIC | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| c1 | 0.09 | 0.127 | 0.16 | 0.004 | 0.005 | 0.006 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.13 | — | 0.23 | 0.005 | — | 0.009 |
| b1 | 0.13 | 0.16 | 0.19 | 0.005 | 0.006 | 0.007 |
| e | 0.40 BSC. | | | 0.016 BSC. | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.07 | | | 0.003 | | |

| | | | |
|---|---|---|---|
| ZI de ROUSSET<br>13106 ROUSSET Cedex<br>FRANCE | **TITLE**<br>**Thin Quad Flat Pack (LQFP),** 128 Pins<br>Body : 14 x 14 x 1.4 mm<br>Foot Print : 2 mm<br>Pitch : 0.4 mm | **Package designation**<br>R-LQ128_G | **REV.**<br>**B** |

# 7. Electrical Characteristics

## 7.1. Absolute Maximum Ratings(*)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Temperature under bias | - | -55 | - | +125 | °C |
| Storage temperature | - | -65 | - | +150 | °C |
| Voltage on: X1, USB_X1 | - | -0.3 | - | VD18+.3 | V |
| MEM pins, TEST0-1,PDWN/ | - | -0.3 | - | VD33+.3 | V |
| 5VT pins | - | -0.3 | - | 5.5 | V |
| Supply voltage | VD18 | -0.3 | - | 1.95 | V |
| | VD33 | -0.3 | - | 3.6 | V |
| | VM | -0.3 | - | 3.6 | V |
| Maximum IOL per I/O pin (excepted MEM pins) | - | - | - | 10 | mA |
| Maximum IOH per I/O pin (excepted MEM pins) | - | - | - | 10 | mA |
| Maximum IOL per I/O MEM pin | - | - | - | 10 | mA |
| Maximum IOH per I/O MEM pin | - | - | - | 10 | mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

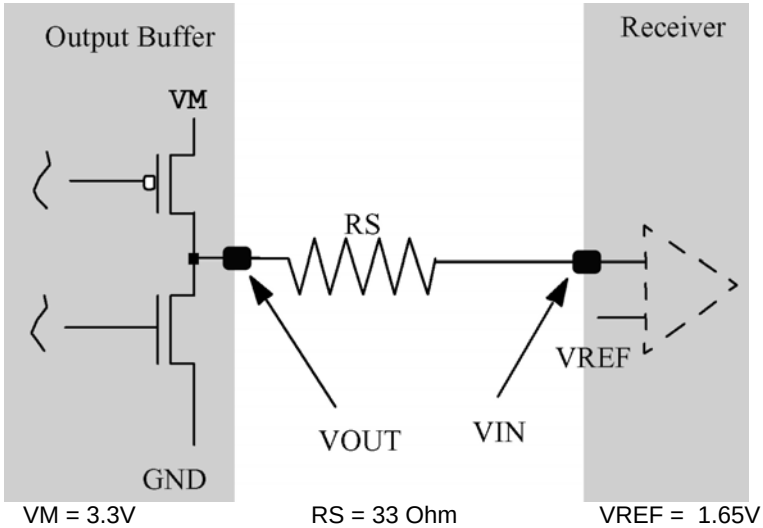
## 7.2. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | VD18 | 1.65 | 1.8 | 1.95 | V |
| Supply voltage | VD33 | 3 | 3.3 | 3.6 | V |
| Operating ambient temperature | tA | 0 | - | 70 | °C |

### 7.2.1. Memory pads

Memory pads (MEM) of SAM3416 are SSTL_2 and LVTTL compliant.
Output drive of memory pads can be selected by firmware between Low (Class1) or High (Class 2).

Note
Default setting is High drive output. However it is recommended to switch to Low drive output for all standard applications with unterminated output load. High drive output should normally be never used.




VM = 3.3V RS = 33 Ohm VREF = 1.65V

Rs should be implemented close to SAM3416.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | VM | 2,3 | 3.3 | 3.6 | V |
| Reference voltage | VREF | VM/2 - 0.04 | 1.65 | VM/2 + 0.04 | V |
| Serial resistor: Low drive output<br>High drive output | RS<br>RS | 22<br>68 | 33<br>82 | 47<br>100 | Ohm<br>Ohm |

## 7.3. D.C. Characteristics (TA=25°C, VD18=1.8V±10%, VD33=3.3V±10%, VM33=3.3V±10%)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Low level input voltage: 5VT pads<br>MEM pads<br>TEST0-1, PDWN/ | VIL<br>VIL<br>VIL | -0.3<br>-0.3<br>-0.3 | -<br>-<br>- | 0.8<br>0.8<br>0.8 | V<br>V<br>V |
| High level input voltage: 5VT pads<br>MEM pads<br>TEST0-1, PDWN/ | VIH<br>VIH<br>VIH | 2<br>2<br>2 | -<br>-<br>- | 5.5<br>3.6<br>3.6 | V<br>V<br>V |
| Low level output voltage: 5VT pads, IOL=8mA<br>MEM pads, IOL=8mA | VOL<br>VOL | -<br>- | -<br>- | 0.4<br>0.4 | V<br>V |
| High level output voltage: 5VT pads, IOH=8mA<br>MEM pads, IOH=8mA | VOH<br>VOH | VD33-0.4<br>VM-0.4 | -<br>- | -<br>- | V<br>V |
| VD18 power supply current (crystal freq.=12.288 MHz, high speed PLL) | ID18 | - | 4 | - | mA |
| VD33 power supply current (crystal freq. = 12.288 MHz, high speed PLL, all P24 stopped, warm Active Power-Down) | ID33 | - | 5.5 | - | mA |
| VD33 deep power down supply current (PDWN/=0) | ID33 | - | 500 | - | µA |
| VD33 power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 stopped) | ID33 | | 77 | | mA |
| VD33 power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 running) | ID33 | | 190 | 240 | mA |
| VM power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 stopped) | IDM | - | 15 | - | mA |
| VM power supply current (crystal freq.= 12.288 MHz, high speed PLL, all P24 running) | IDM | - | 20 | - | mA |
| Built-in pull-up / pull-down resistor | PU/PD | 30 | 50- | 100 | kOhm |

# 8. Peripherals and Timings

A built-in PLL multiplies the Xtal clock frequency by 4 or 6 for internal use. plck is the period of the internal clock generated by PLL. plck = tck/4 or tck/6. Typical values with Xtal 12.288 MHz are plck = 20 ns or 13.6 ns.

## 8.1. LCD display interface

Pin used: DB8-DB0 (I/O), RS (output), RW (output), ENB (output)
All signals are controlled by P16 firmware, therefore their timing relationship is determined by firmware only

## 8.2. Front Panel Scanning interface (Switches, LEDs, Sliders)

Pin used: SEL0 (I/O), ROW2-ROW0 (I/O), BR7-BR0 (I/O), MK7-MK0 (I/O), VIN
All signals are controlled by P16 and/or P24, therefore their timing relationship is determined by firmware only.

## 8.3. EEPROM / DataFlash interface

This is a master synchronous serial interface, operating in SPI mode 0.

Pins used:
DFSI, DFSCK (outputs)
DFSO (input)

The DFSCK frequency is firmware programmable from fck/4 to fck/256, fck being the system clock frequency (fck=1/plck). This allows accommodating a large variety of EEPROM/DataFlash devices.

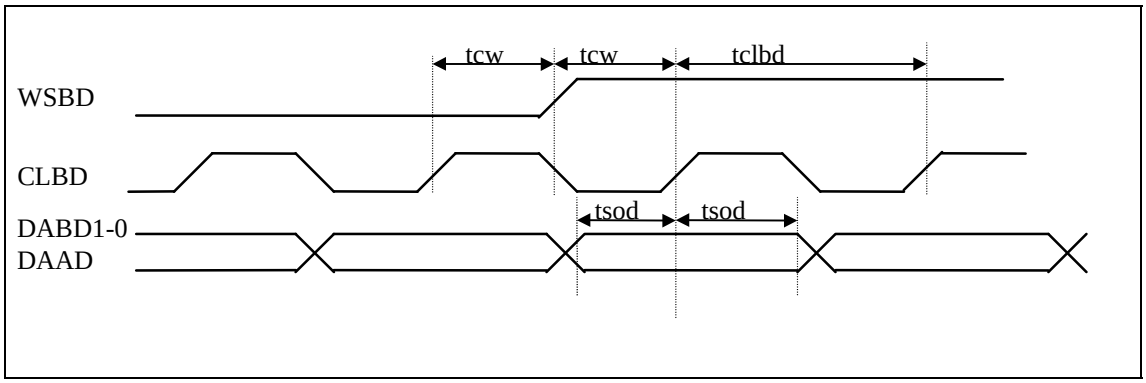
Please refer to Atmel DataFlash datasheets for accurate SPI mode 0 timing.

## 8.4. Digital audio

Pins used:
CLBD, WSBD (outputs)
DABD1-0 (outputs)
DAAD (input)

The SAM3416 allows for 4 digital audio output channels and 2 digital audio input channels. All audio channels are synchronized on single clocks CLBD, WSBD which are derived from the IC crystal oscillator.

The digital audio timing follows the I2S or MSB left standard, with up to 24 bits per sample




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CLBD rising to WSBD change | tcw | tc-10 | - | - | ns |
| DABD valid prior/after CLBD rising | tsod | tc-10 | - | - | ns |
| CLBD cycle time | tclbd | - | 2*tc | - | ns |

tc is related to plck as follows:

| Sample freq WSBD | tc | CLBD/WSBD freq ratio |
|---|---|---|
| 1/(plck*512) | 4*plck | 64 |
| 1/(plck*768) | 8*plck | 48 |
| 1/(plck*1024) | 8*plck | 64 |
| 1/(plck*1536) | 16*plck | 48 |

Frame Format (FMT) is the number of plck cycles per digital audio frame. FMT is configurable by firmware. Possible values are: 512, 768, 1024, 1536

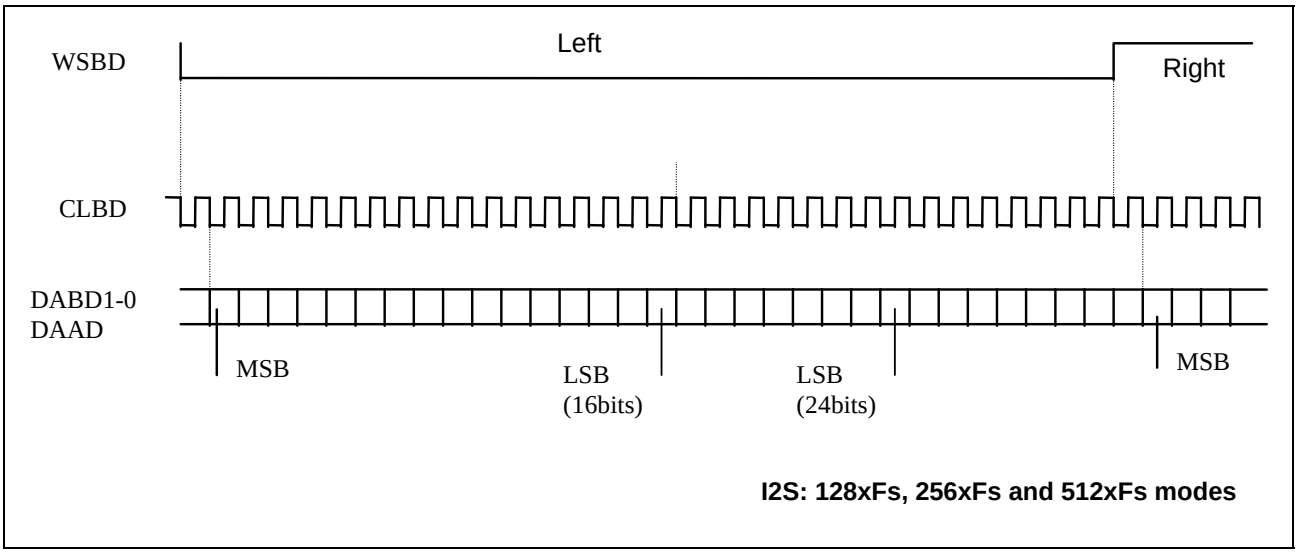
The choice of clock factors is done by the firmware. plck factor can have two values (see note below). Speed option allows single or double speed mode for CKOUT. As an example, table below show all possible clock combinations with 12.288MHz Xtal.

| plck value | CKOUT Speed | FMT | CKOUT/WSBD freq ratio | CLBD/WSBD freq ratio | fs @ Xtal=12.288MHz |
|---|---|---|---|---|---|
| tck/4 | Single | 1536 | 384 | 48 | 32kHz |
| **tck/4** | **Single** | **1024** | **256** | **64** | **48kHz** |
| tck/4 | Single | 768 | 192 | 48 | 64kHz |
| **tck/4** | **Single** | **512** | **128** | **64** | **96kHz** |
| tck/4 | Double | 1536 | 768 | 48 | 32kHz |
| **tck/4** | **Double** | **1024** | **512** | **64** | **48kHz** |
| tck/4 | Double | 768 | 384 | 48 | 64kHz |
| **tck/4** | **Double** | **512** | **256** | **64** | **96kHz** |
| **tck/6** | **Single** | **1536** | **384** | **48** | **48kHz (default)** |
| tck/6 | Single | 1024 | 256 | 64 | 72kHz |
| **tck/6** | **Single** | **768** | **192** | **48** | **96kHz** |
| tck/6 | Single | 512 | 128 | 64 | 144kHz |
| **tck/6** | **Double** | **1536** | **768** | **48** | **48kHz** |
| tck/6 | Double | 1024 | 512 | 64 | 72kHz |
| **tck/6** | **Double** | **768** | **384** | **48** | **96kHz** |
| tck/6 | Double | 512 | 256 | 64 | 144kHz |

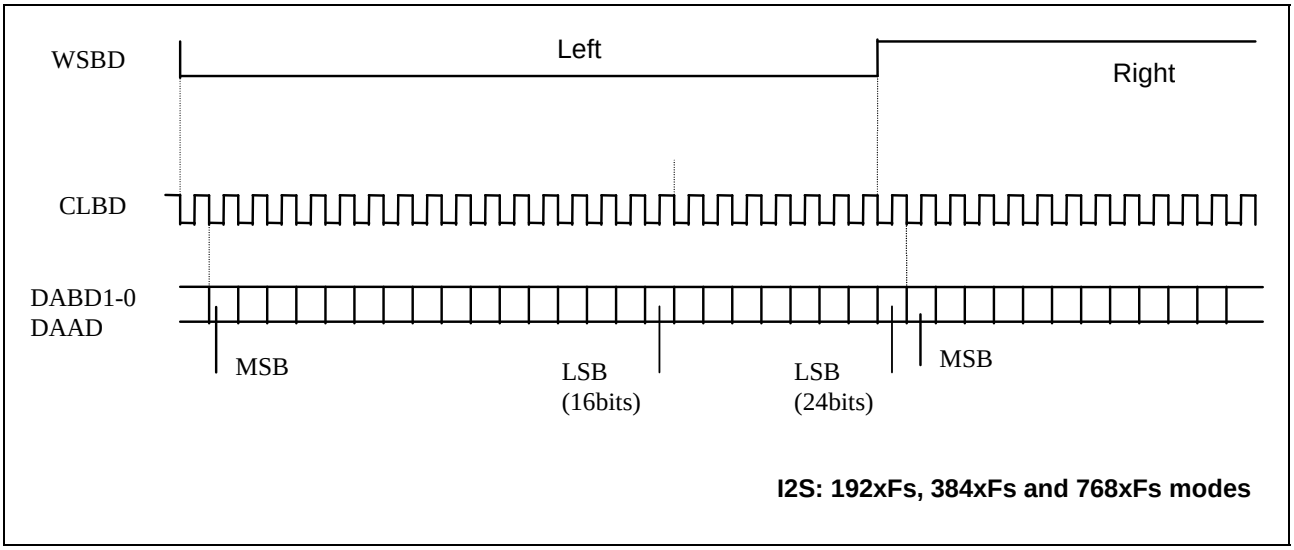
Note: For use with standard DREAM firmware/library only plck value = tck/6 can be used, with FMT=3 (48KHz).
CKOUT speed can be single or double, defined by firmware

## DIGITAL AUDIO FRAME FORMAT

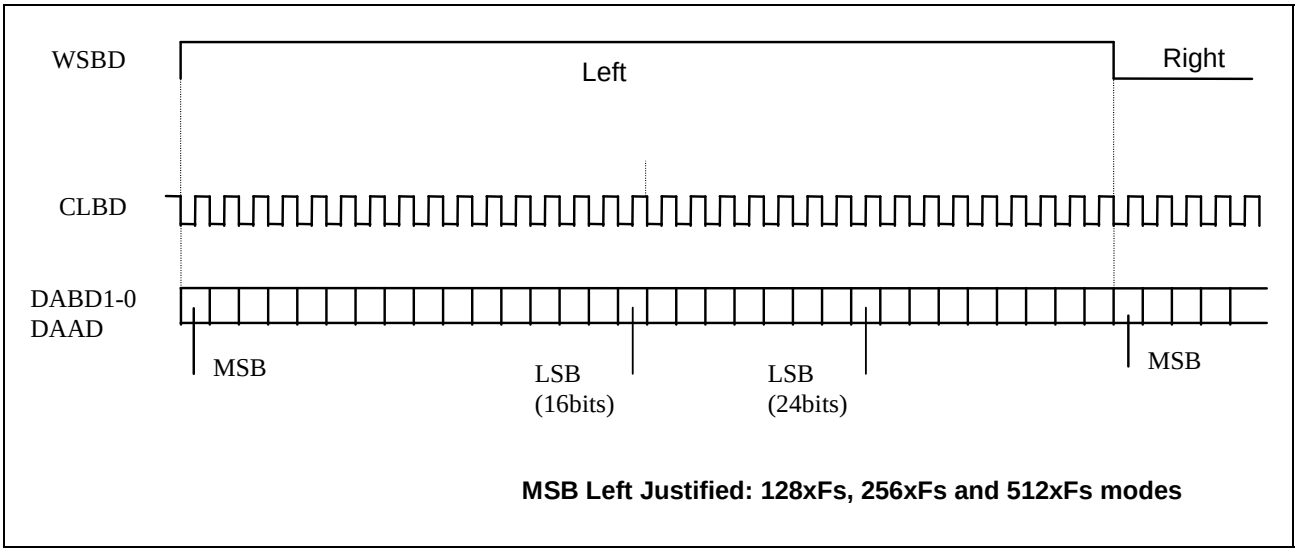
SAM3416 can generate I2S or MSB Left justified digital audio format. Master Clock can be 128xFs, 256xFs, 512xFs, 192xFs, 384xFS or 768xFs. Format and clock ratio are selected by firmware.



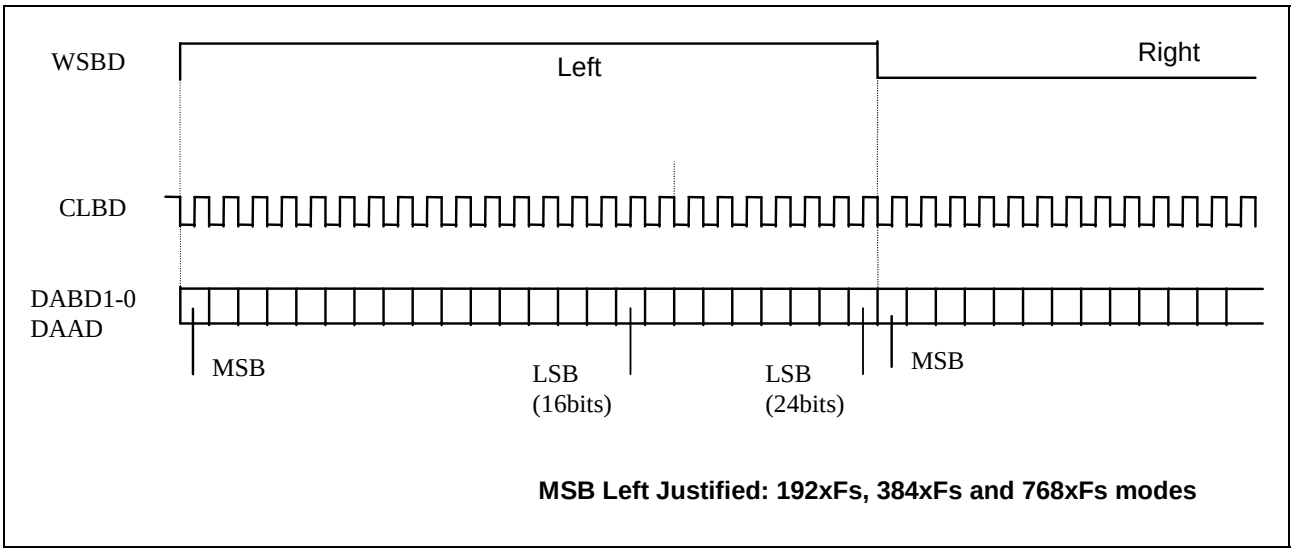

**I2S: 128xFs, 256xFs and 512xFs modes**




**I2S: 192xFs, 384xFs and 768xFs modes**




**MSB Left Justified: 128xFs, 256xFs and 512xFs modes**




**MSB Left Justified: 192xFs, 384xFs and 768xFs modes**

## 8.5. Serial MIDI_IN and MIDI_OUT

The serial MIDI IN and OUT signals are asynchronous signals following the MIDI transmission standard:

baud rate: programmable, typically 31.25 kb/s.
format: start bit(0), 8 data bits, stop bit(1)

## 8.6. NOR Flash, ROM and RAM external memory

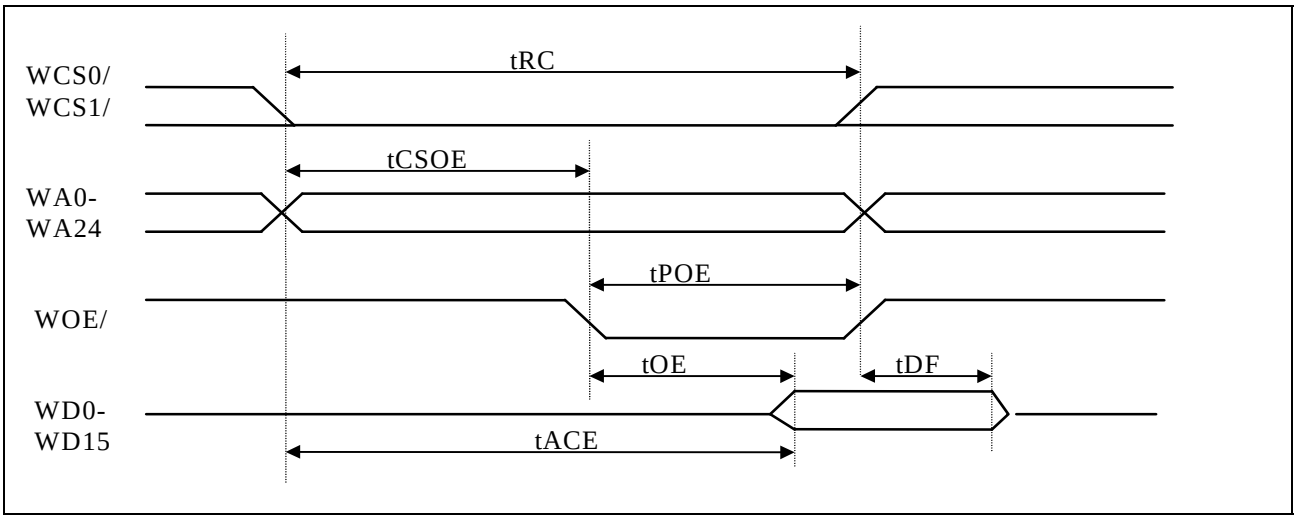
Pins used:

WA24-WA0: address out
WD15-WD0: data bi-directional
WCS0/ or XCS11/, XCS02/
WCS1/

WOE/: output enable
WWE/: write

When using all address bits, the maximum addressing range is two pages (WCS0/, WCS1/) of 32M words (total = 128 Mbytes).

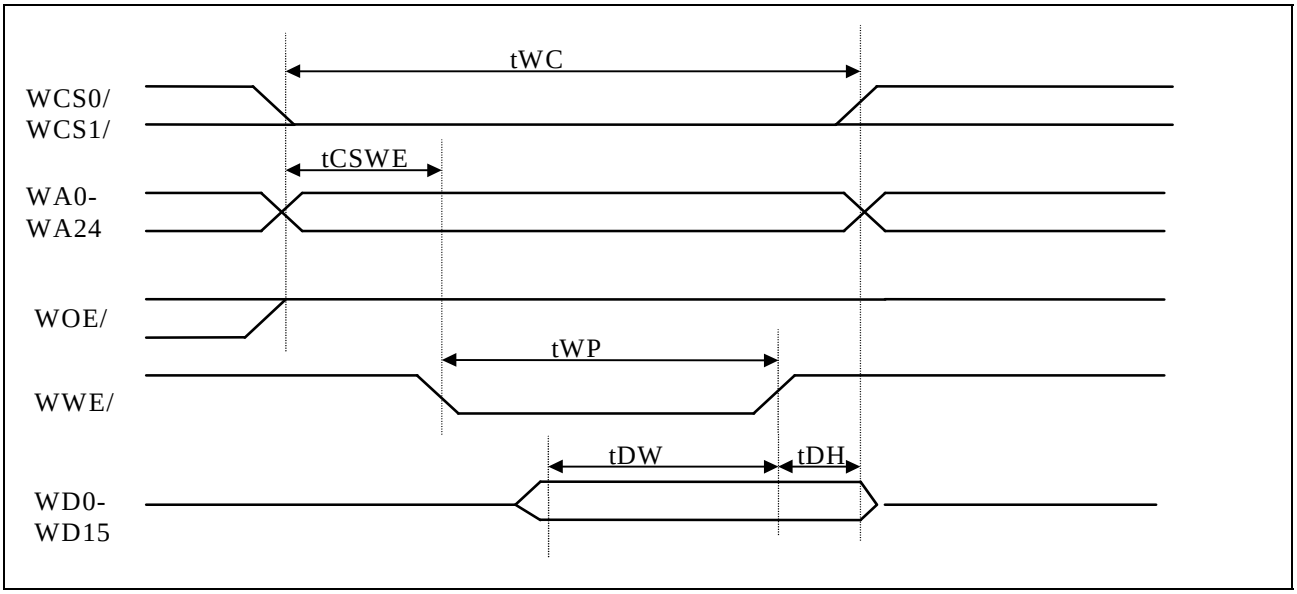
ROM/Flash READ CYCLE




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Read cycle time | tRC | N*plck-5 | N*plck | N*plck+5 | ns |
| Chip select low / address valid to WOE/ low | tCSOE | 1*plck-5 | 1*plck | 1*plck+5 | ns |
| Output enable pulse width | tPOE | (N-1)*plck-5 | (N-1)*plck | (N-1)*plck+5 | ns |
| Chip select/address access time | tACE | (N-0.5)*plck-5 | - | - | ns |
| Output enable access time | tOE | (N-1,5)*plck-5 | - | - | ns |
| Chip select or WOE/ high to input data Hi-Z | tDF | 0 | - | 1*plck | ns |

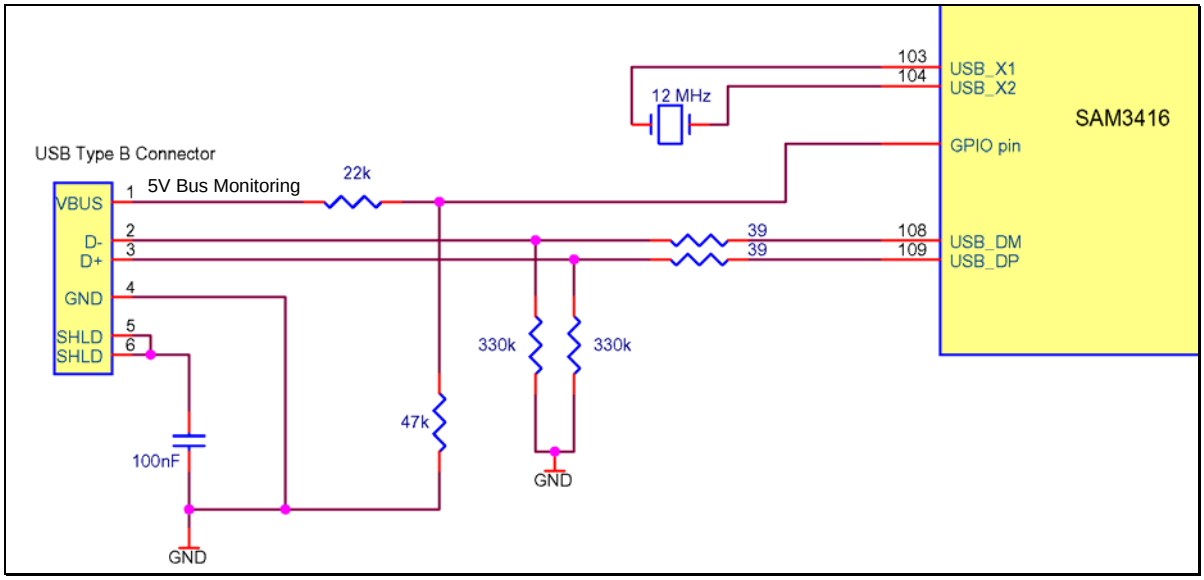
Notes:
- N is number of system clock cycles. It can be programmed by firmware from 1 to 8
- Memory access time should be lower than tACEmin.

EXTERNAL RAM/FLASH WRITE TIMING




| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Write cycle time | tWC | N*plck-5 | N*plck | N*plck+5 | ns |
| Write enable low from CS/ or Address or WOE/ | tCSWE | 1*plck-5 | 1*plck | 1*plck+5 | ns |
| Write pulse width | tWP | (N-1)*plck-5 | (N-1)*plck | (N-1)*plck+5 | ns |
| Data out setup time | tDW | (N-1)*plck-5 | - | - | ns |
| Data out hold time | tDH | 0.5*plck-5 | 0.5*plck | 0.5*plck+5 | ns |

## 9. USB Typical Connection




## 10. Reset and Power Down

During power-up, the RESET/ input should be held low until the crystal oscillator and PLL are stabilized, which takes max. 10ms.
After the low to high transition of RESET/, following happens:

- All P24s enter an idle state.
- P16 program execution starts in built-in ROM.

The power-up sequence is as follows:

- STIN is sensed. If HIGH, then the built-in debugger is started.
- Address 0 from internal Flash is checked. If “DR” is read, then control is transferred to address 400H from internal Flash.

If PDWN/ is asserted low, then the crystal oscillator and PLL are stopped. The chip enters a deep power down sleep mode, as power is removed from the core. To exit power down, PDWN/ has to be asserted high, then RESET/ applied.

Other power reduction features allowing warm restart are controlled by firmware:

- P24s can be individually stopped
- The clock frequency can be internally divided by 256

## 11. Recommended Board Layout

Like all HCMOS high integration ICs, following simple rules of board layout is mandatory for reliable operations:

- GND, VD33, VM, VD18 distribution, decoupling

All GND, VD33, VM, VD18 pins should be connected. A GND plane is strongly recommended. The board GND, VD33, VM and VD18 distribution should be in grid form.

Recommended VD18 decoupling is 0.1µF at each VD18 pin of the IC with an additional 10µFT decoupling close to the crystal. Minimum recommended VM decoupling is 0.1µF at each VM pin. VD33 requires a single 0.1µF decoupling.

- Crystal

The paths between the crystal, the crystal compensation capacitors and the IC should be short and shielded. The ground return from the compensation capacitors filter should be the GND plane from the IC.

- Busses

Parallel layout from DB7-DB0 and WA24-WA0/WD15-WD0 should be avoided. The DB7-DB0 bus is an asynchronous type bus. Even on short distances, it can induce pulses on WA24-WA0/WD15-WD0 which can corrupt address and/or data on these busses.

A ground plane should be implemented below the WA24-WA0/WD15-WD0 bus, which connects both to the Flash and RAM grounds and to the IC.

## 12. Product development and debugging

Dream provides an integrated product development and debugging tool SamVS. SamVS runs under Windows (XP, Vista, Win7, Win8). Within the environment, it is possible to:

- Edit
- Assemble
- Debug on real target (In Circuit Emulation)
- Program internal or external Flash, DataFlash, EEPROM on target.

Two dedicated IC pins, STIN and STOUT allow running firmware directly into the target using standard PC COM port communication at 57.6 kbauds. Thus time to market is optimized by testing directly on the final prototype.

A library of frequently used functions is available such as:

- Effects: Reverb, Chorus, Flanger, Phaser, Delay, Distortion, Pitch shifter…
- Audio Processing: EQ, Filter, Compressor, Limiter, Noise-Gate, Vocoder…
- Functions: Pitch Detection, Feedback canceller…
- MIDI Synthesis
- MP3 Decode
- and many more

Dream engineers are available to study customer specific applications.

**Dream Contact**

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